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Project Code & Schematics Subject: H901 Main Board_6L

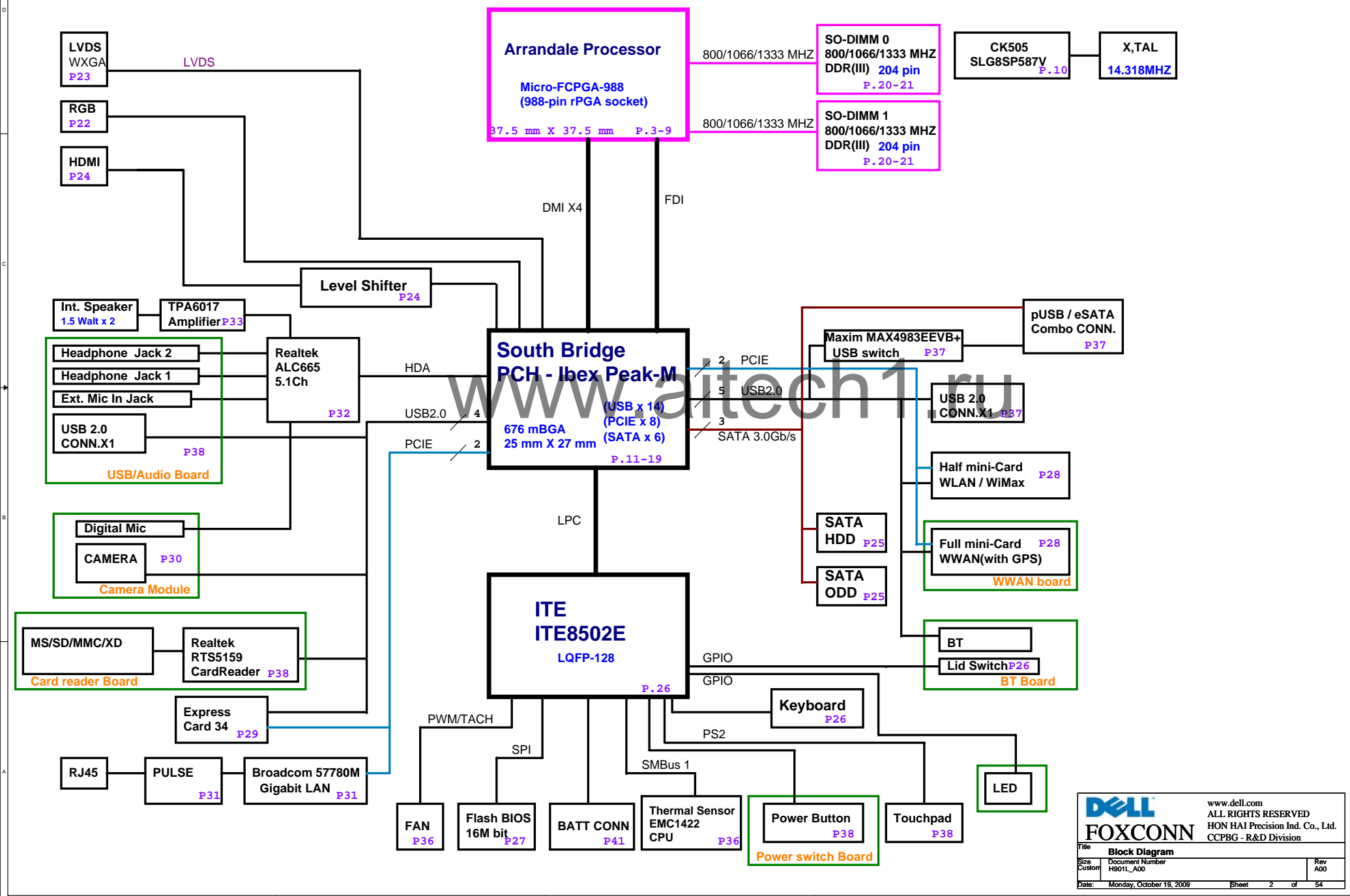
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LED DB P/N:	1P-1099J02-6000 (IRIS)
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P/B DB P/N:	1P-1099J00-6000 (IRIS)
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	1P-1099202-6000 (NANYA)

P. Leader	Check by	Design by

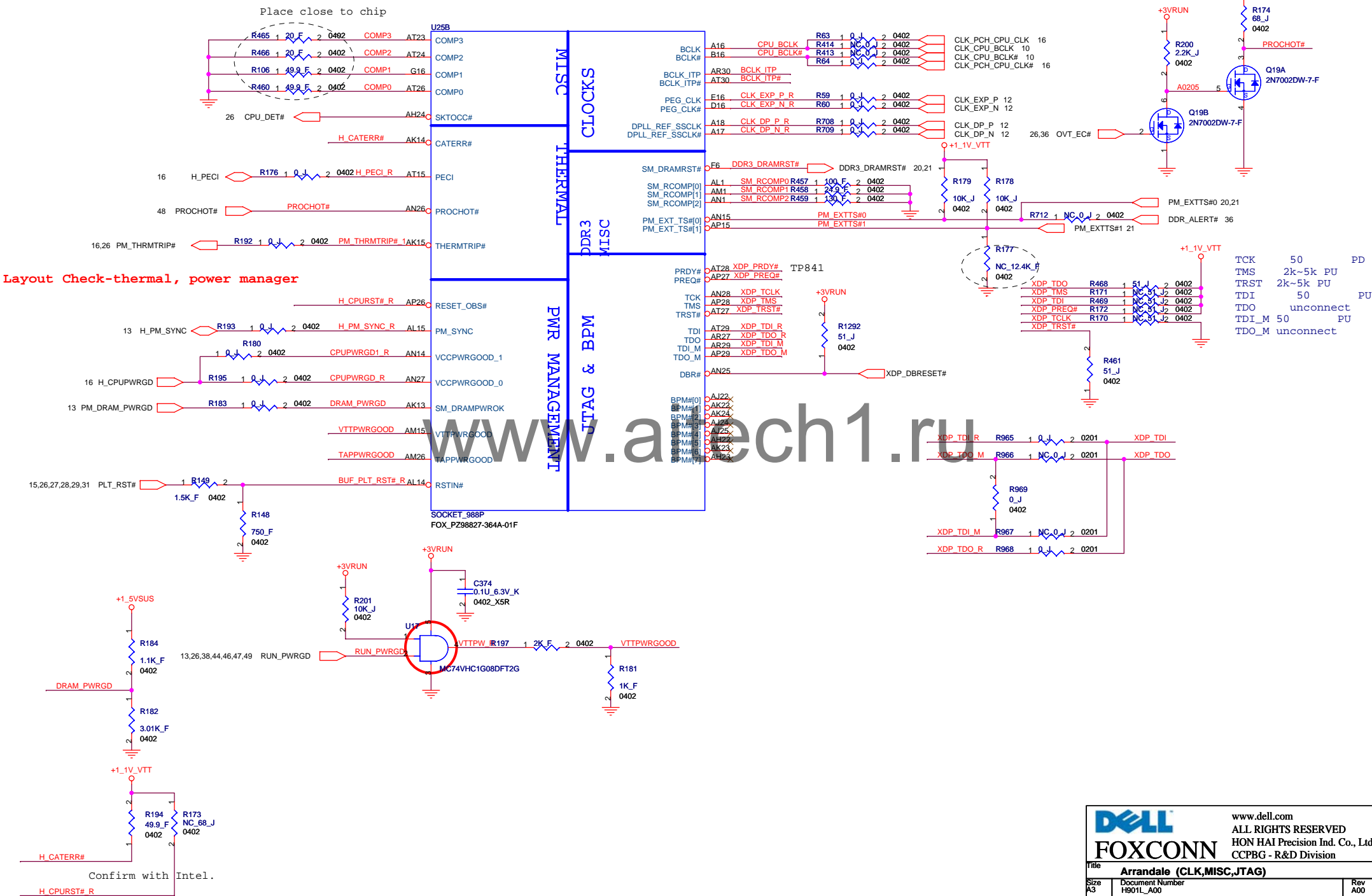
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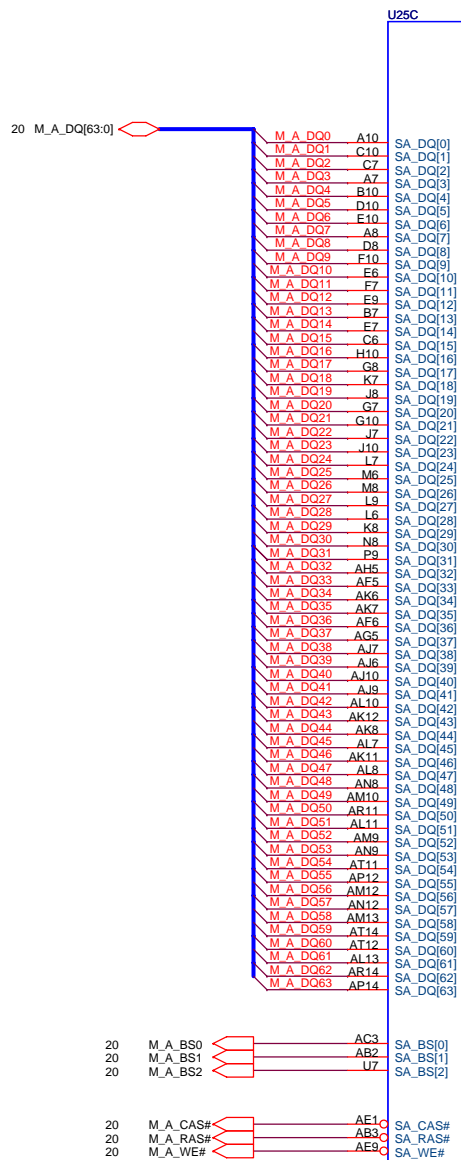
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H901L Arrandale

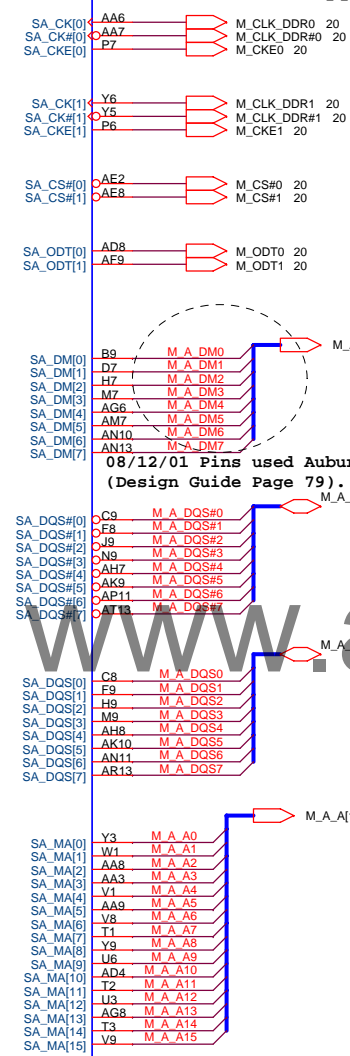


Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

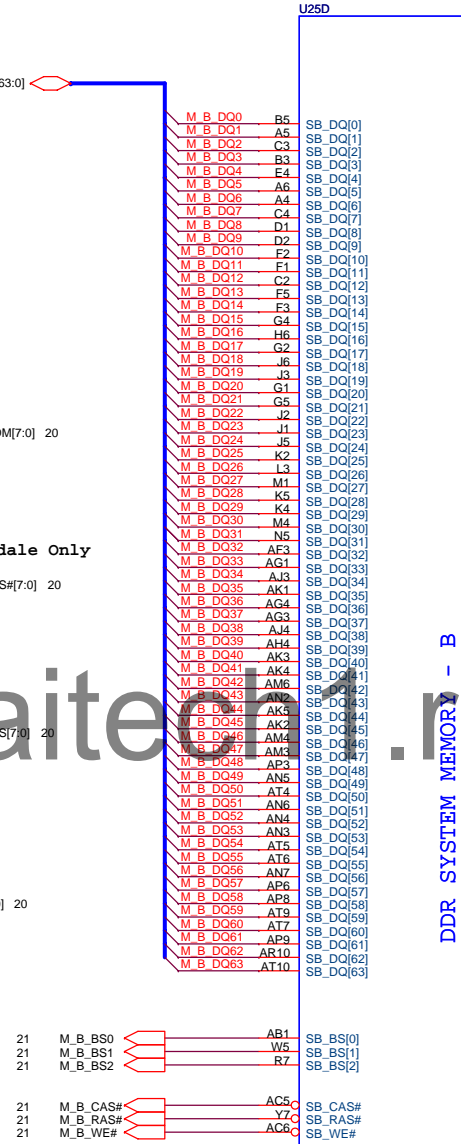




DDR SYSTEM MEMORY A

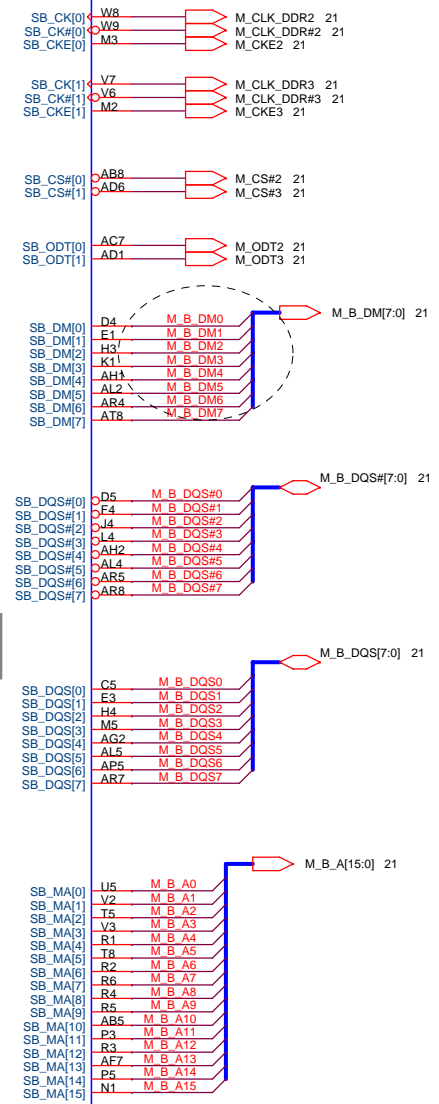



SOCKET_988P
FOX_PZ98827-364A-01F



DDR SYSTEM MEMORY B

SOCKET_988P
FOX_PZ98827-364A-01F





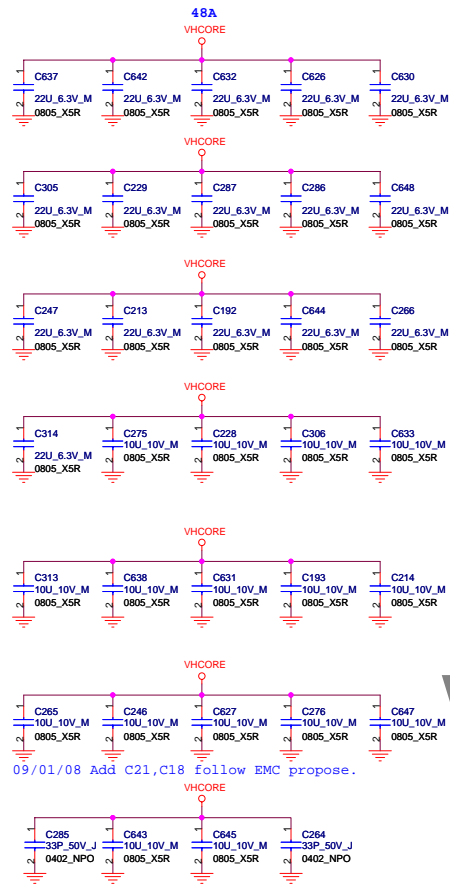
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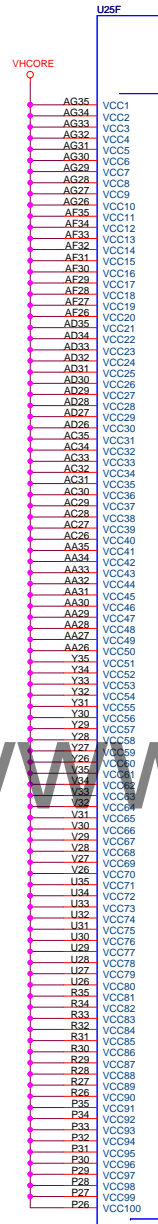
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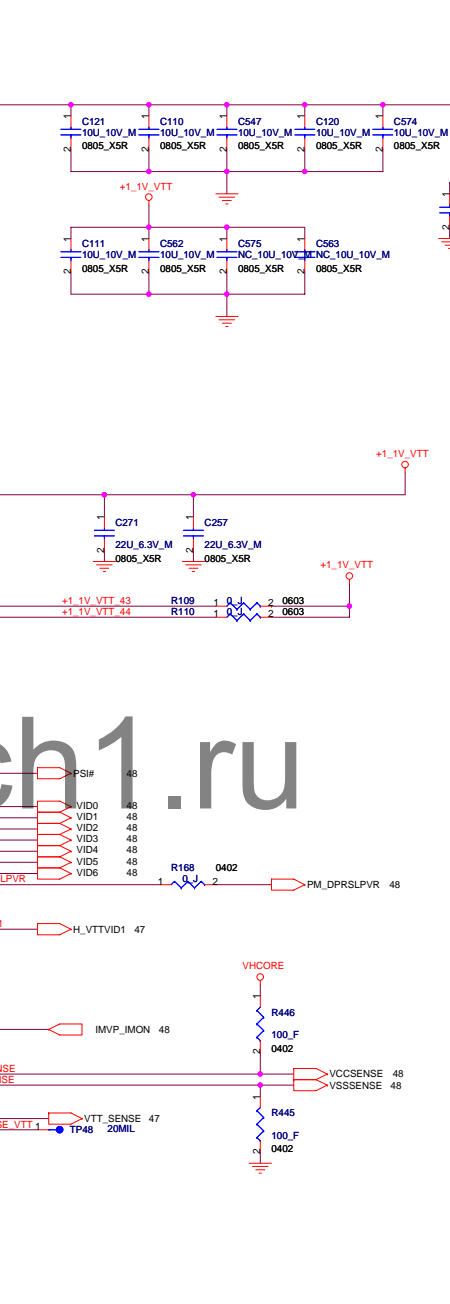
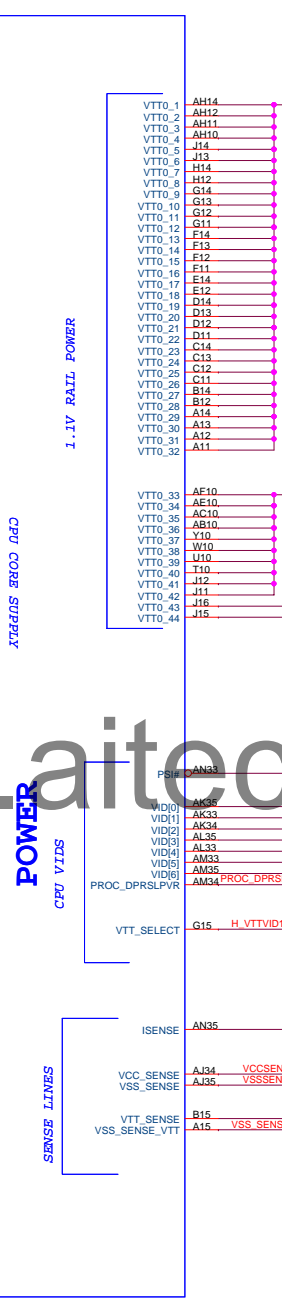
Date: Monday, October 19, 2009 Sheet 5 of 54



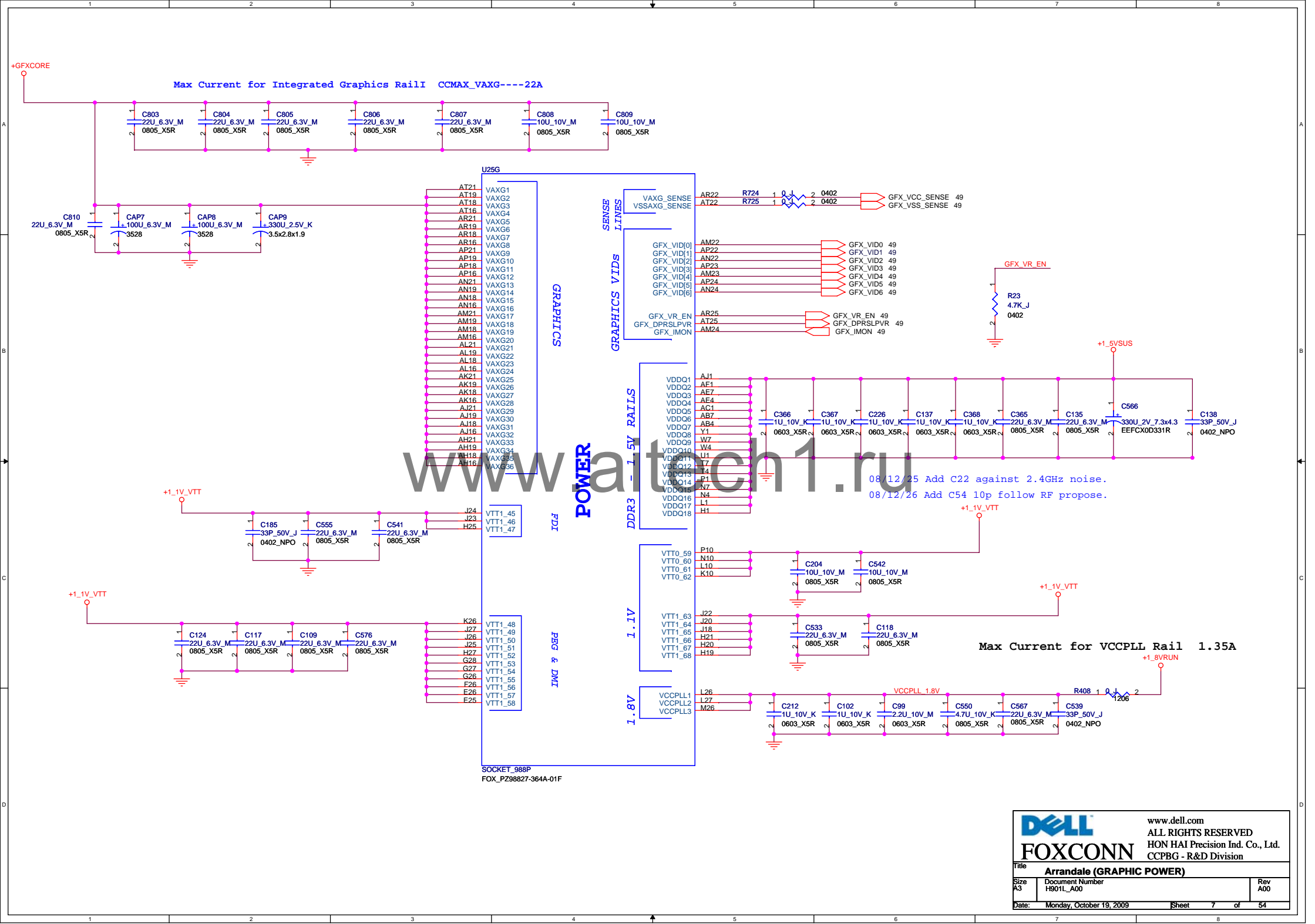
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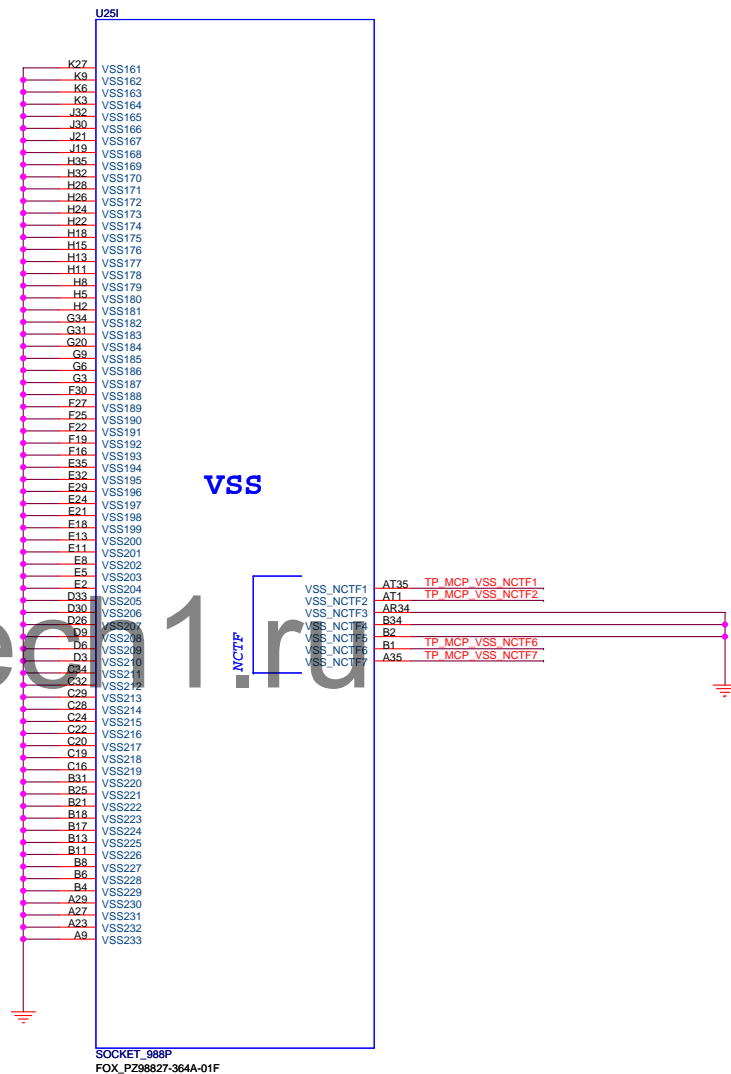
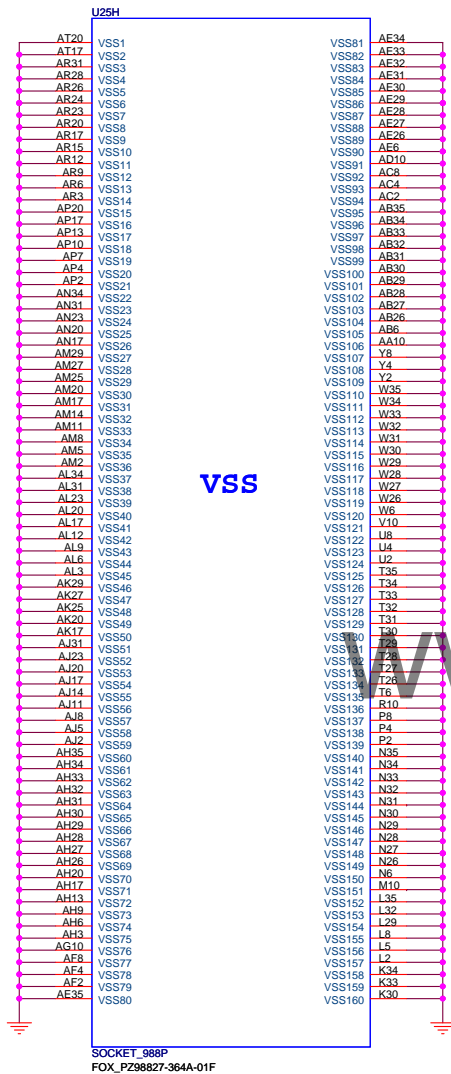


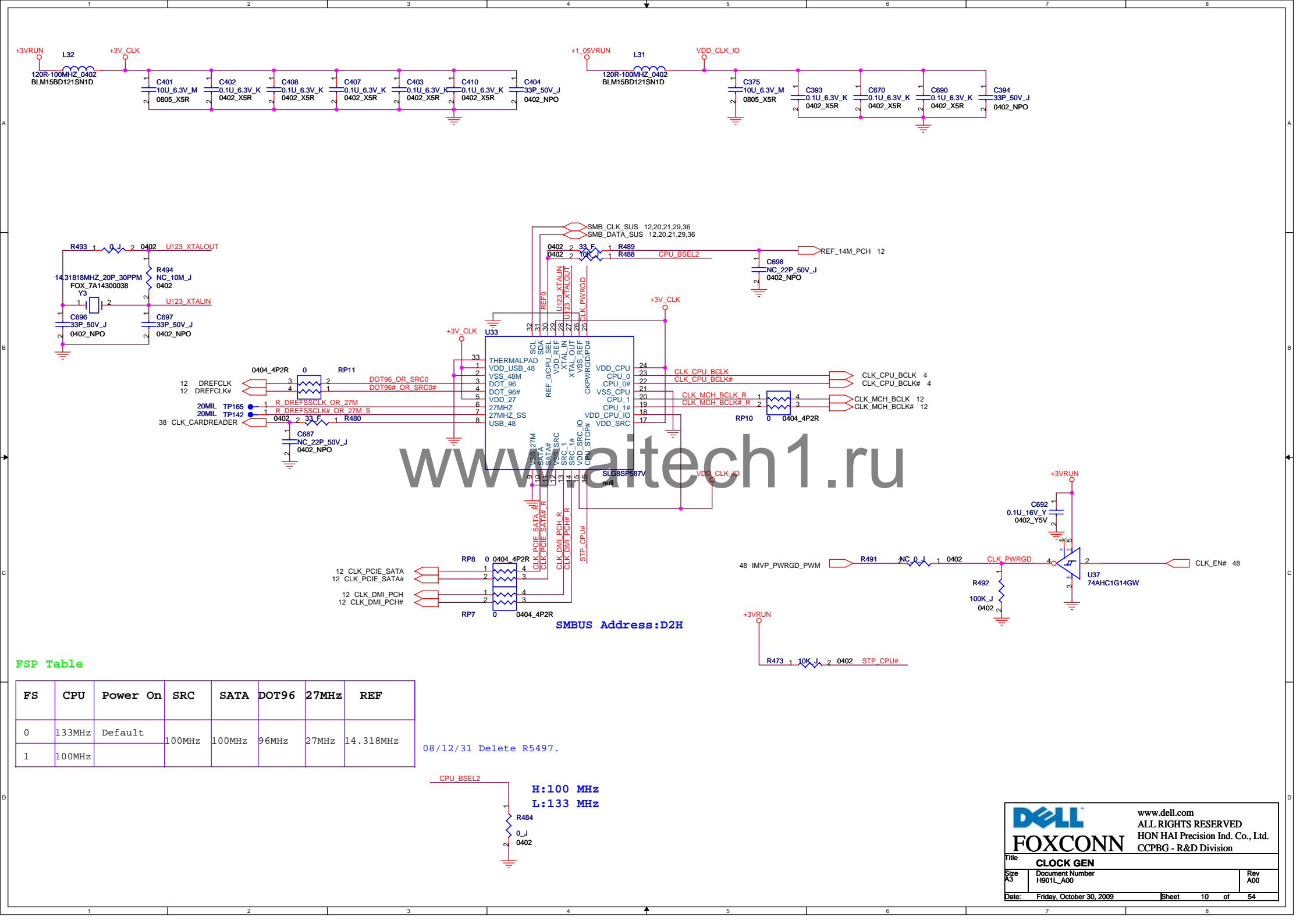
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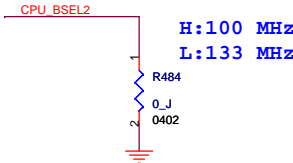





FSP Table

FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

08/12/31 Delete R5497.





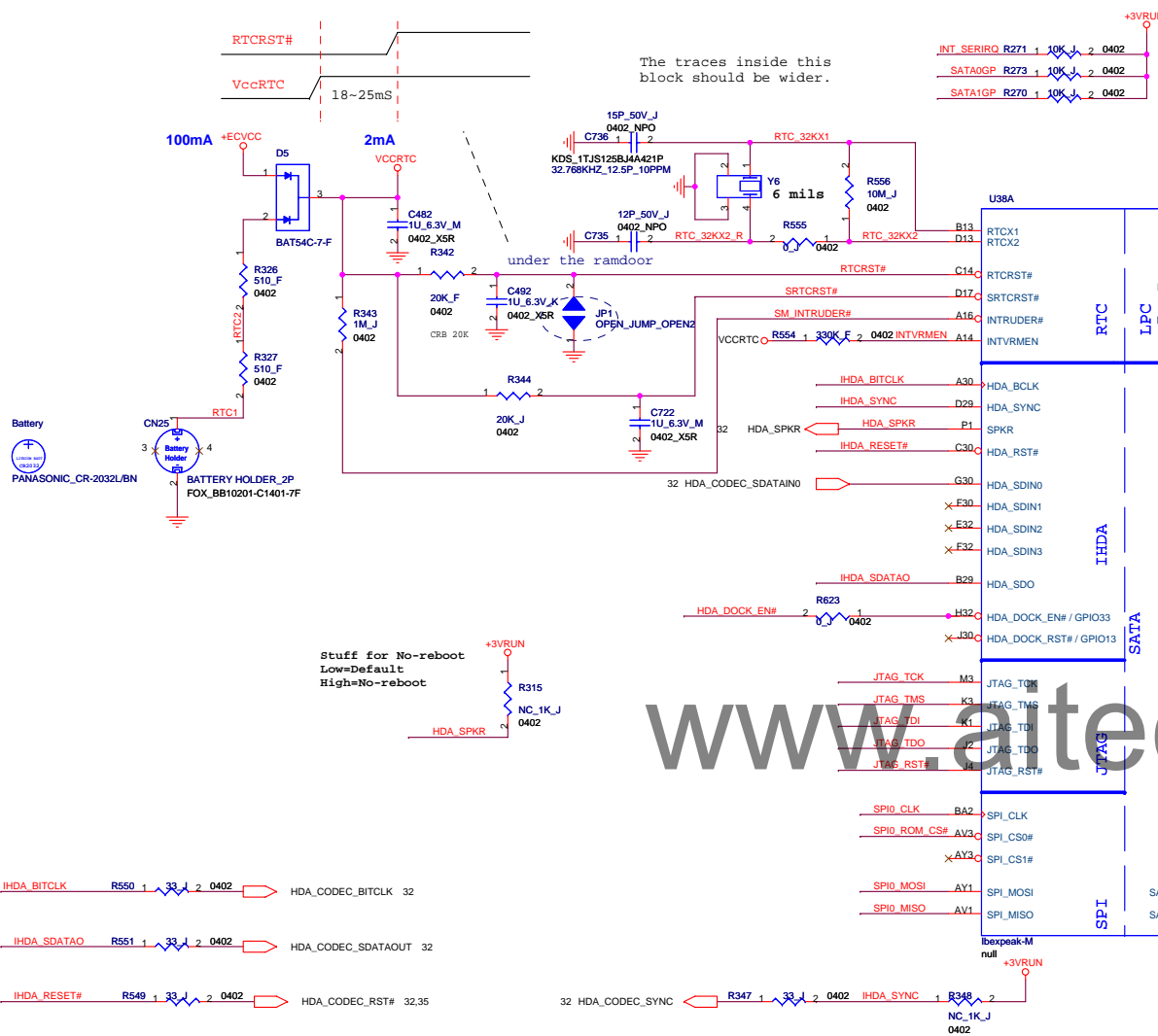
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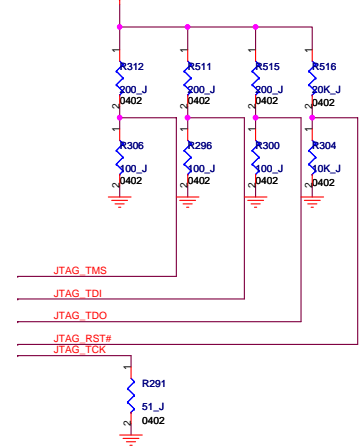
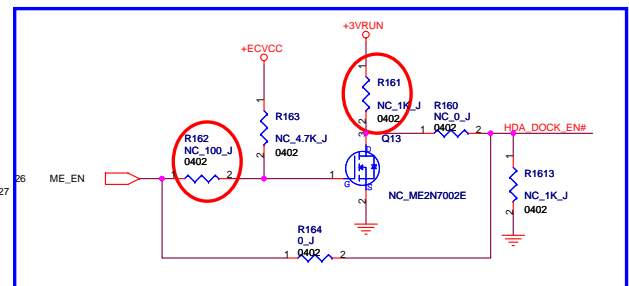
Title: **CLOCK GEN**

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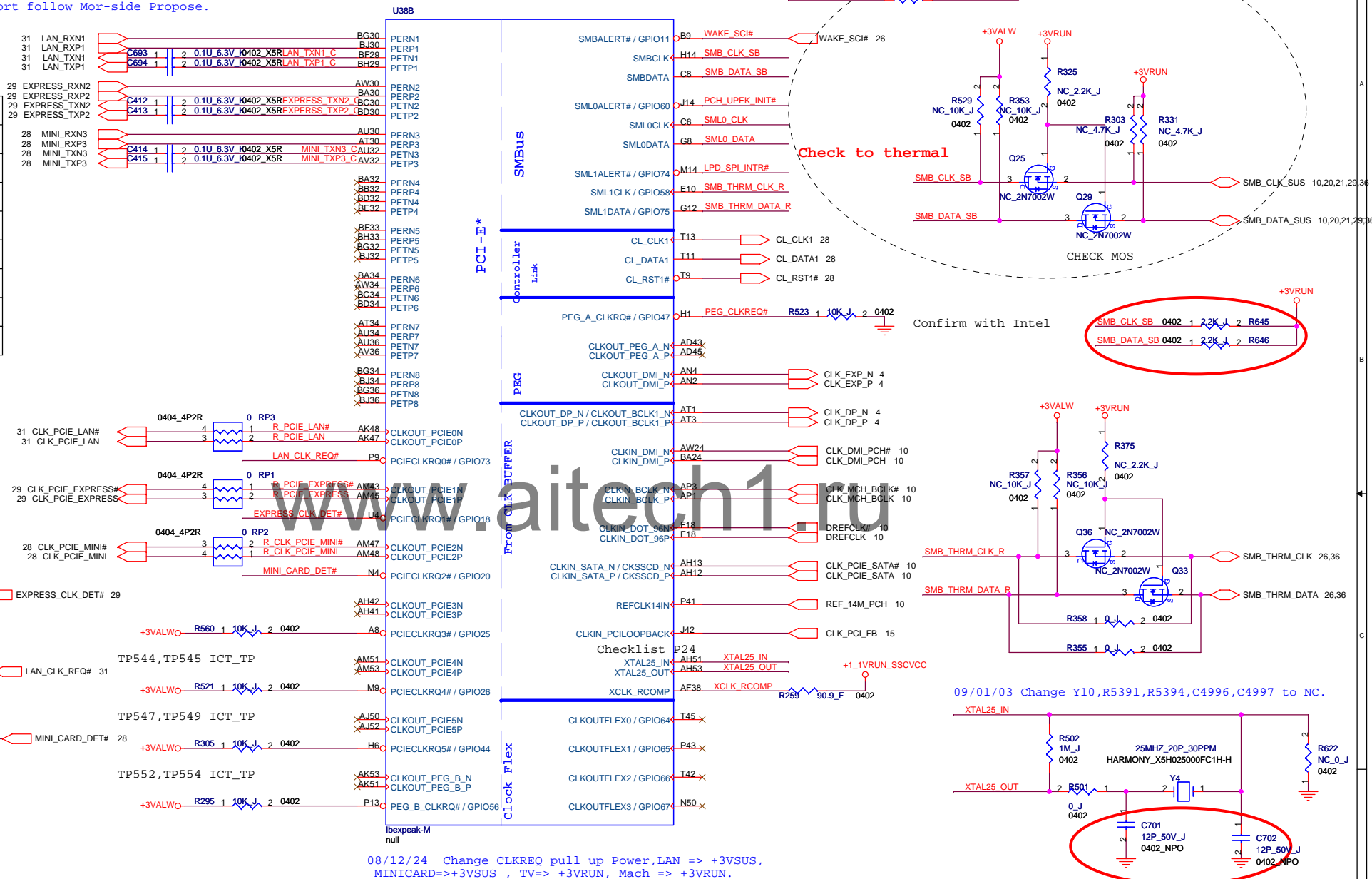


[HDA_DOCK_EN#/GPIO33]
Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) - Security measure defined in the Flash Descriptor will be enabled

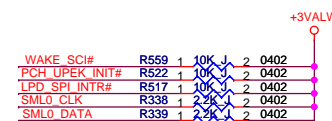


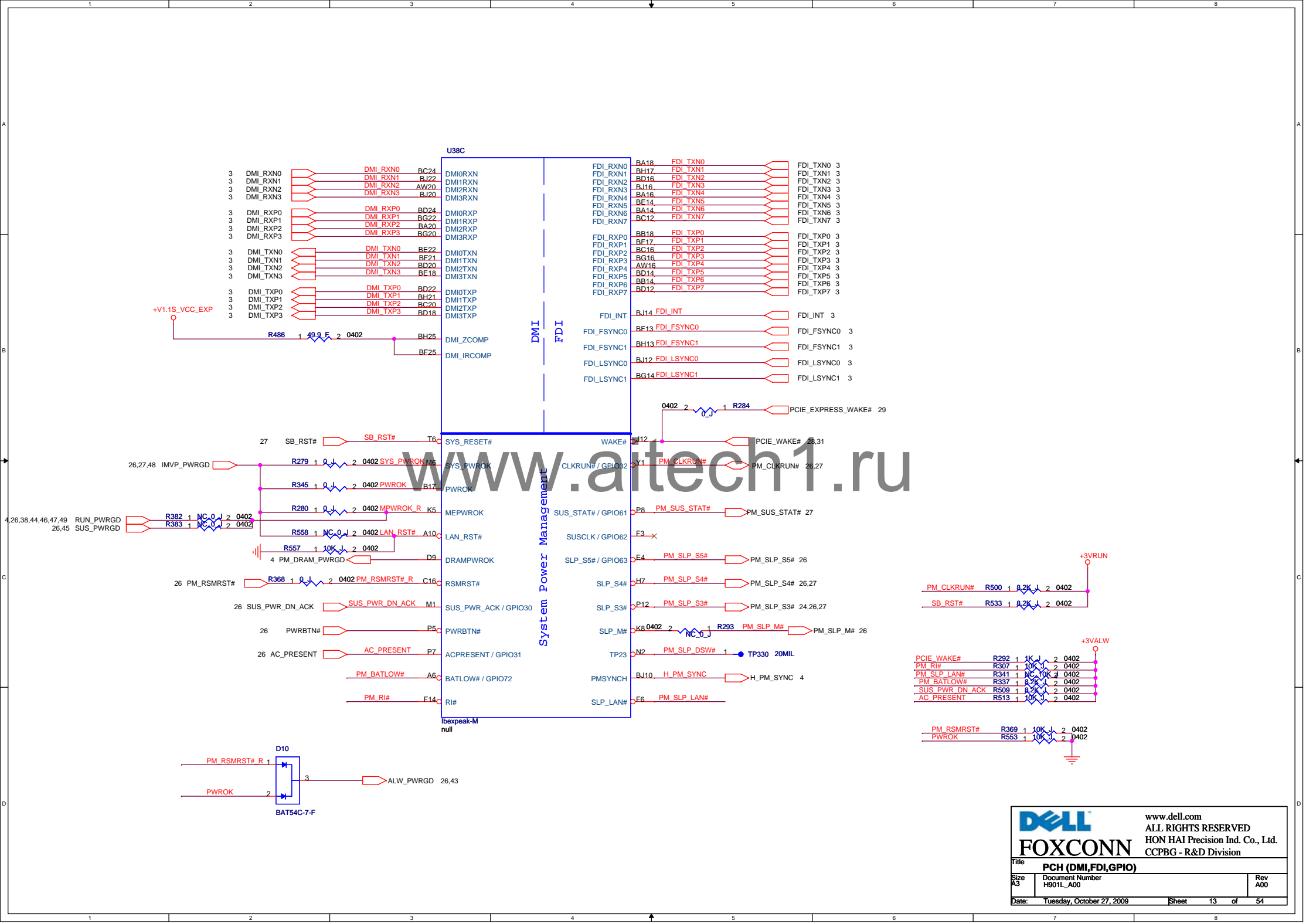
PCI-E Port Table

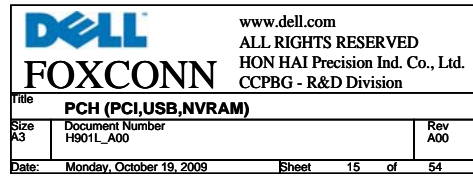
Port	Function
Port1	LAN
Port2	Express Card
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

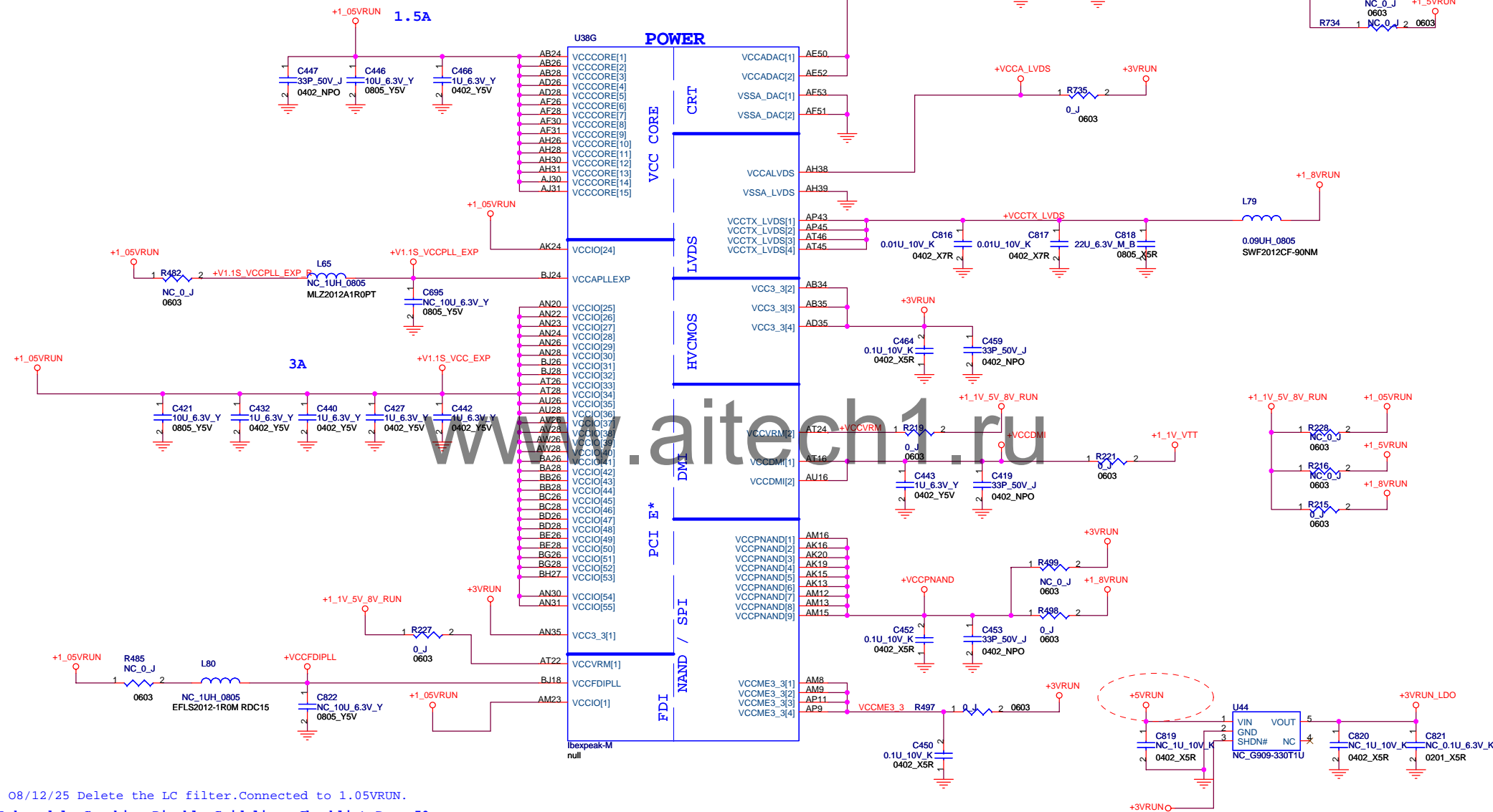


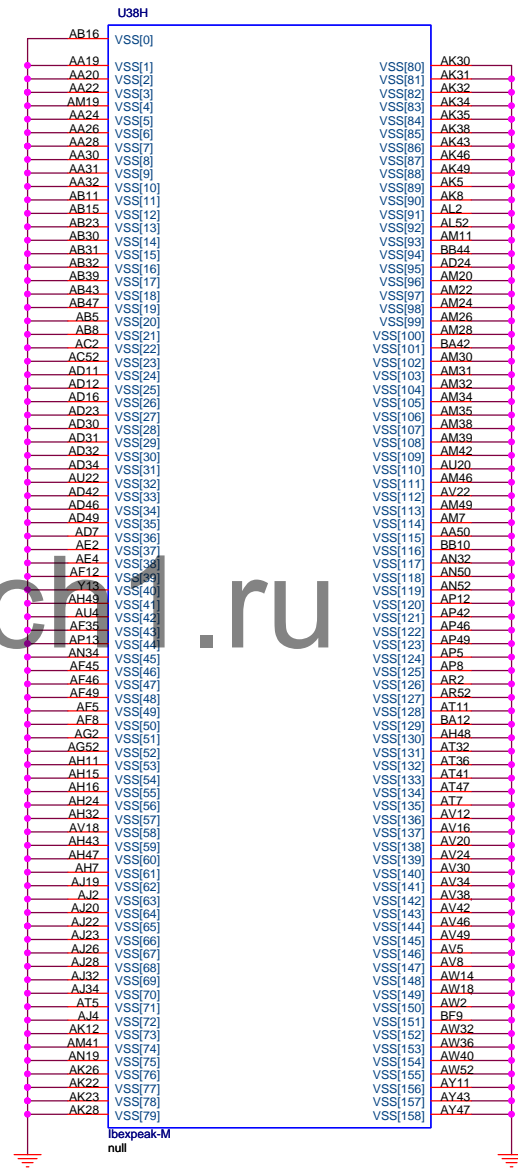
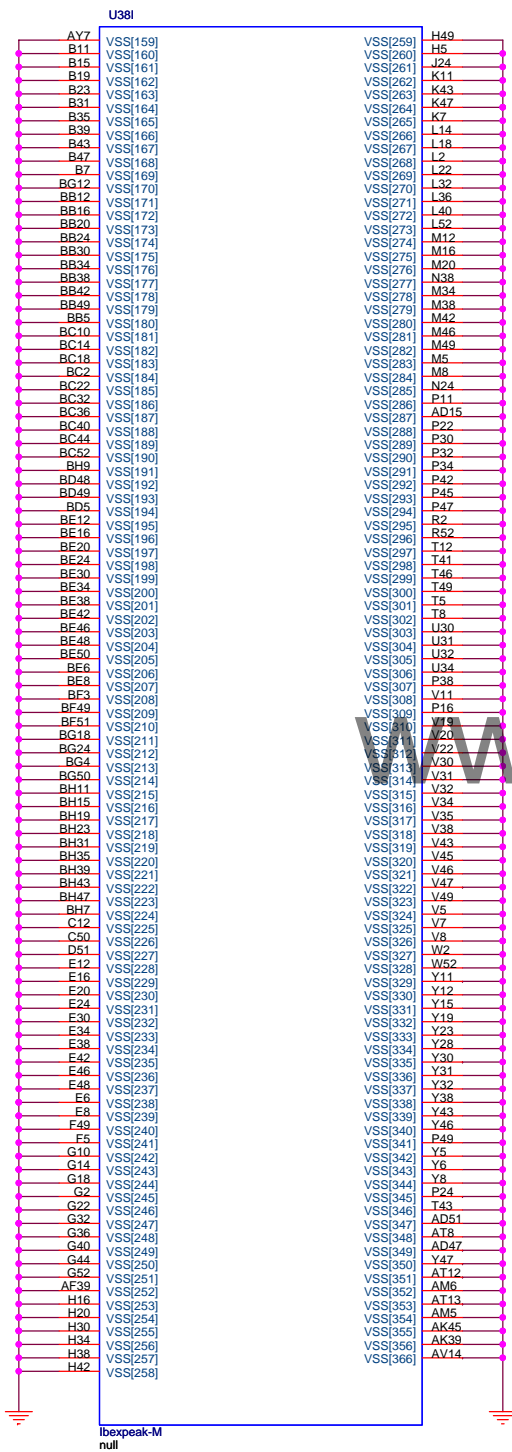
08/12/24 Change CLKREQ pull up Power, LAN => +3VSUS,
MINICARD=>+3VSUS , TV=> +3VRUN, Mach => +3VRUN.







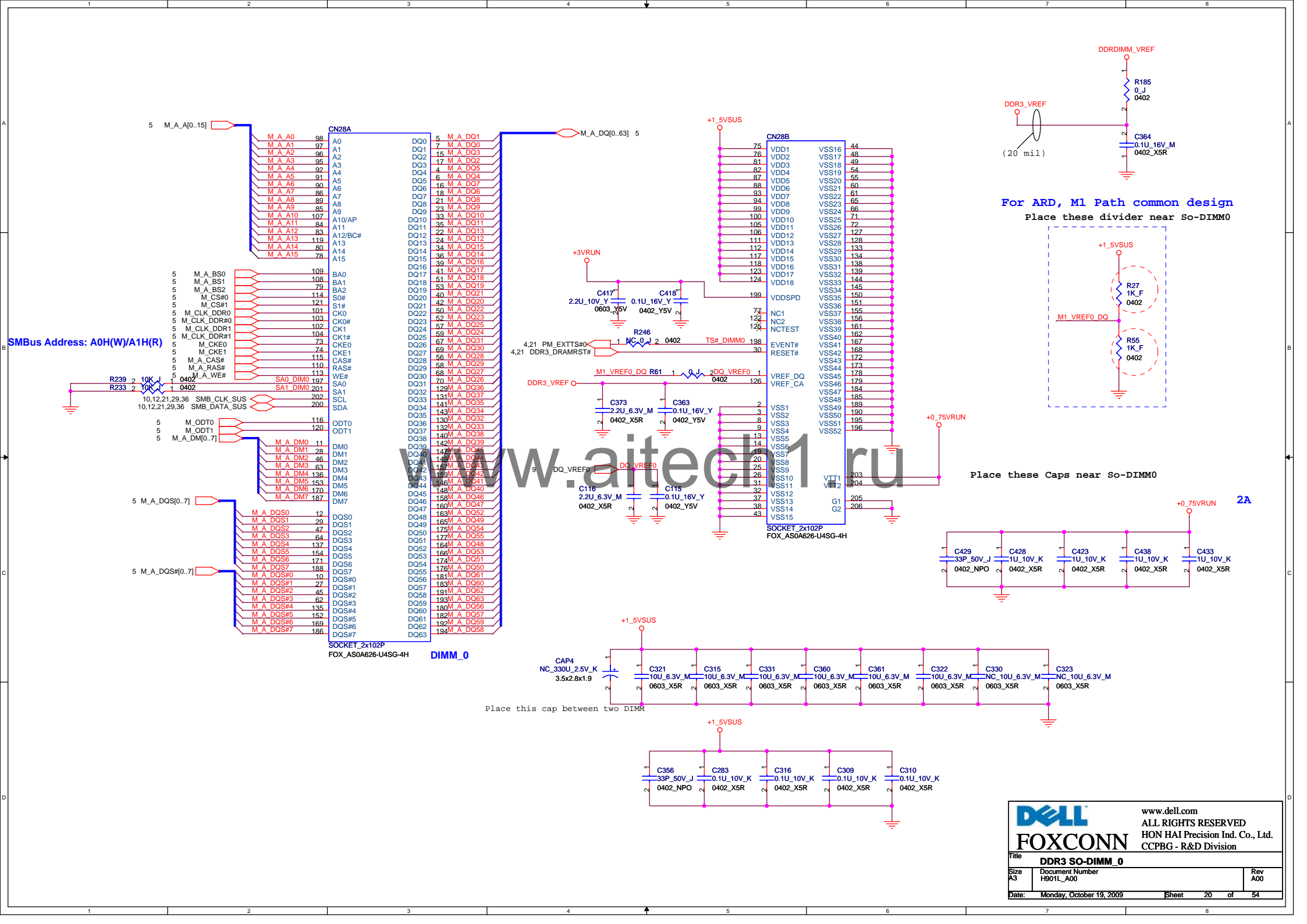


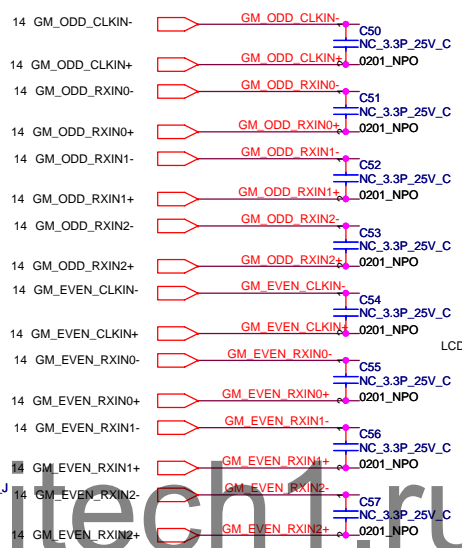
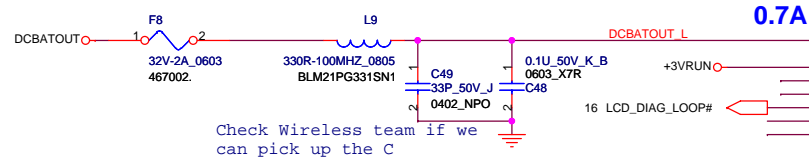
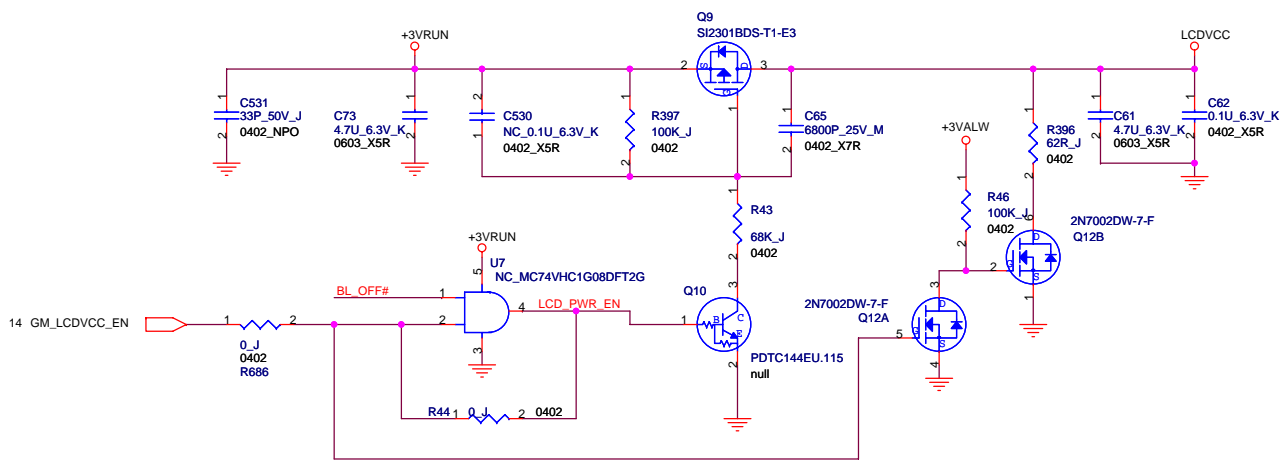
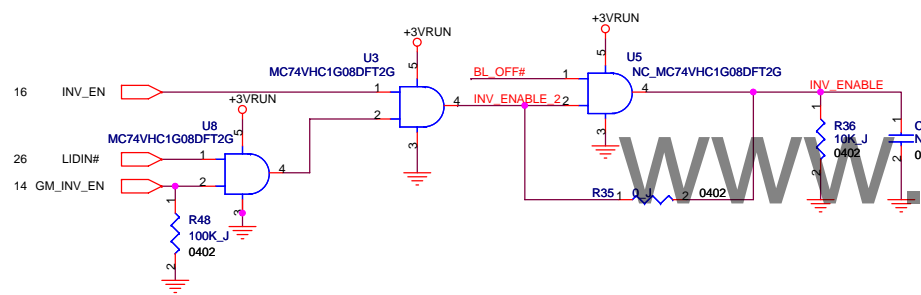
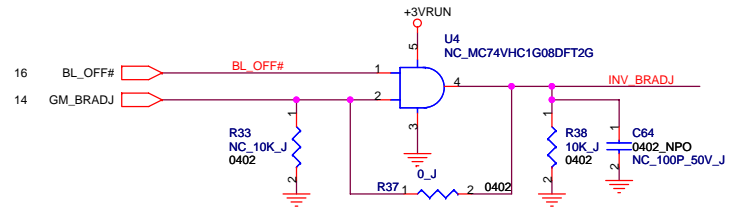


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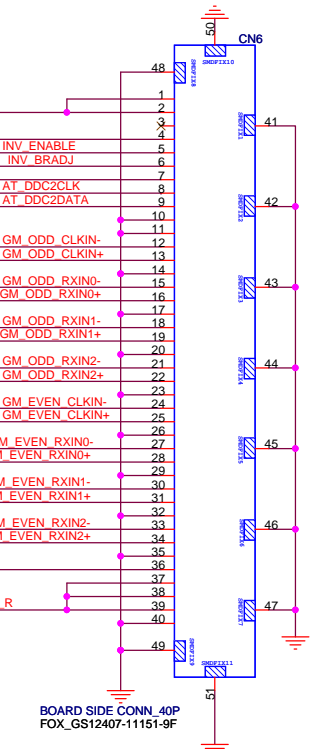
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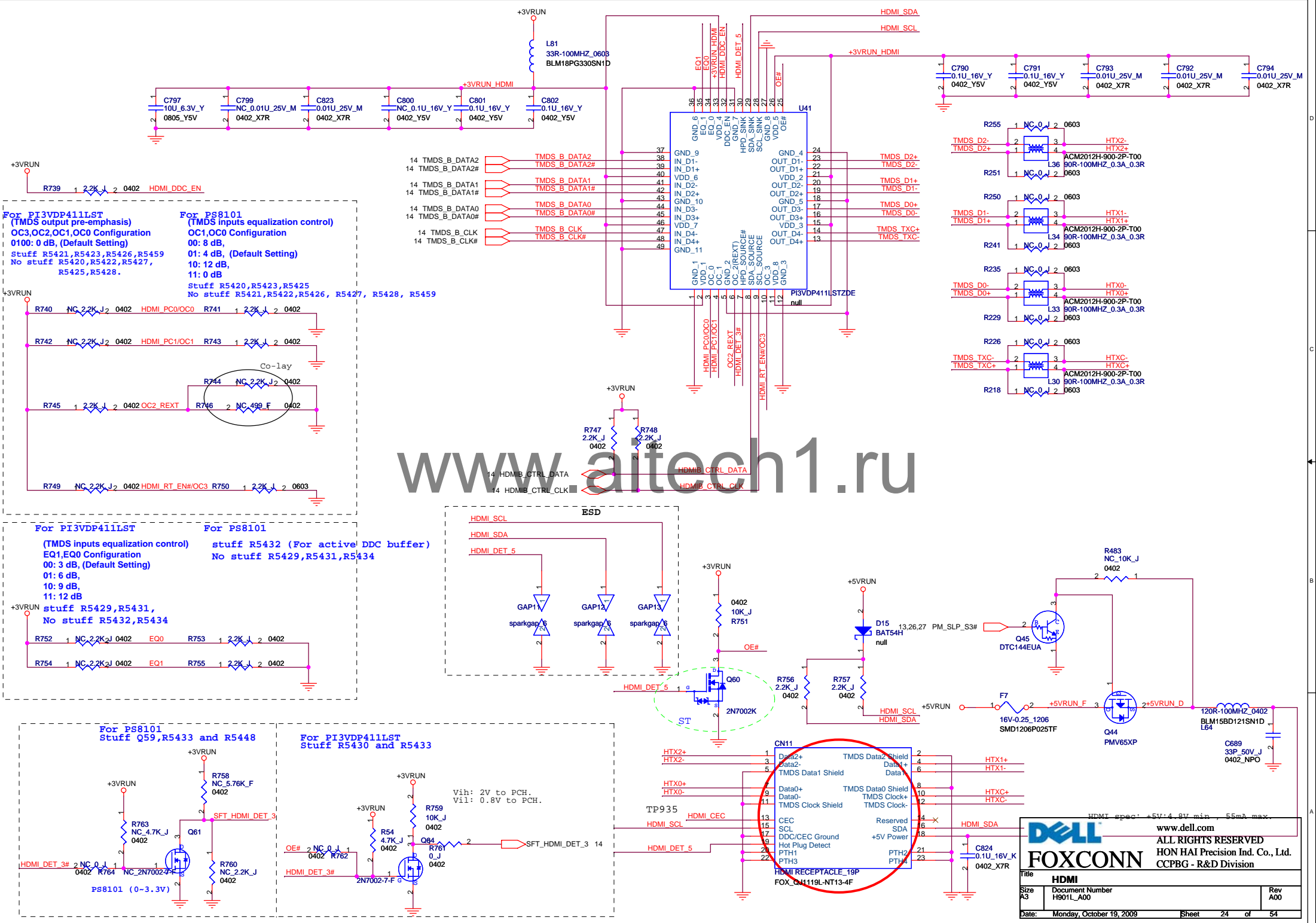




0.7A



Pin 4 +3VRUN change to Pin 10 in DVT.



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HDMI spec: +5V: 4.8V min, 55mA max.

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DELL

FOXCONN

Title: **HDMI**

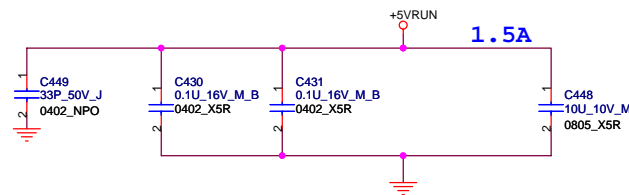
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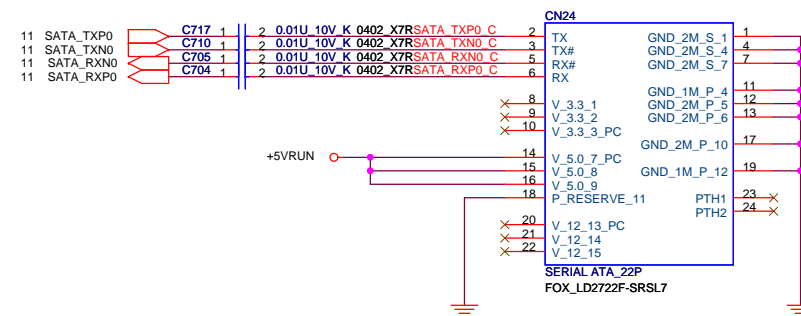
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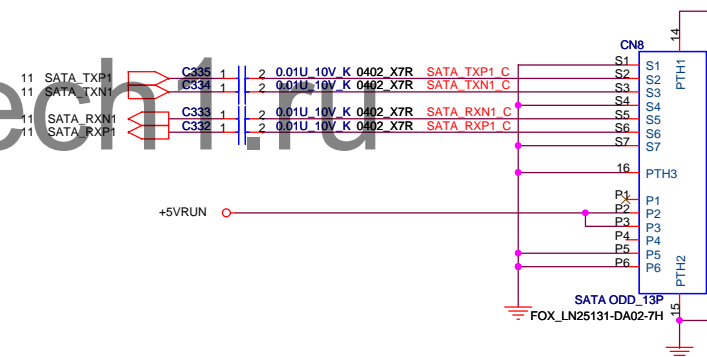
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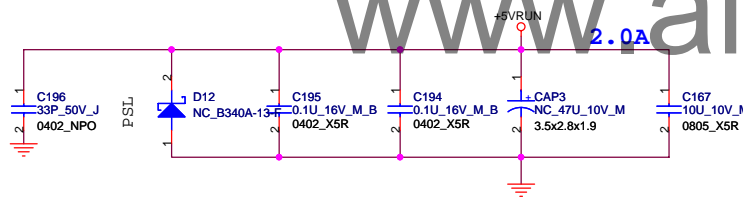


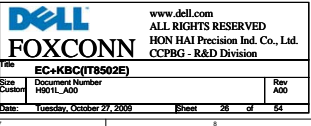
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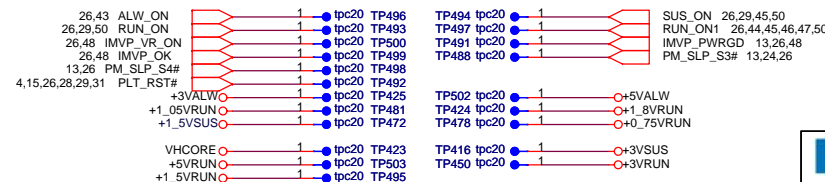
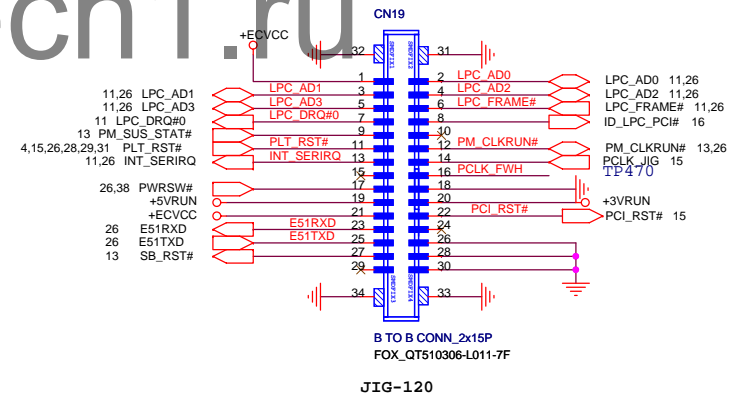
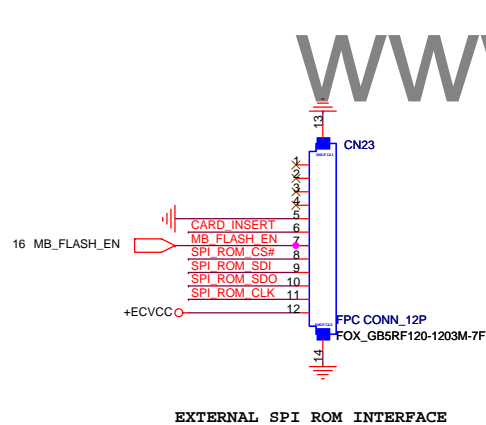
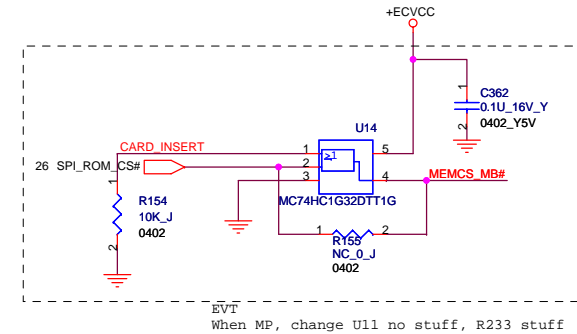
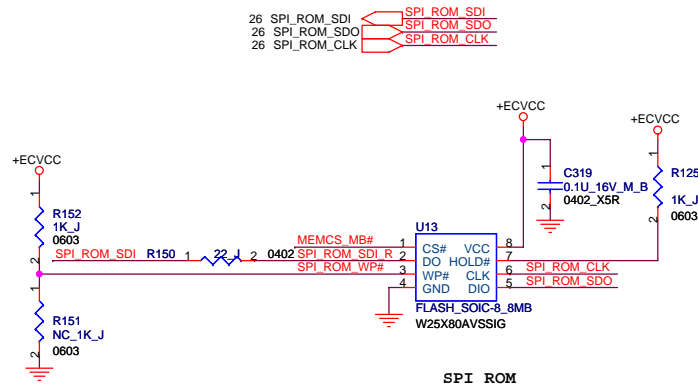


ODD CON ADAPTER

Add CN68 need 2N-0013009-FKG0 in BOM

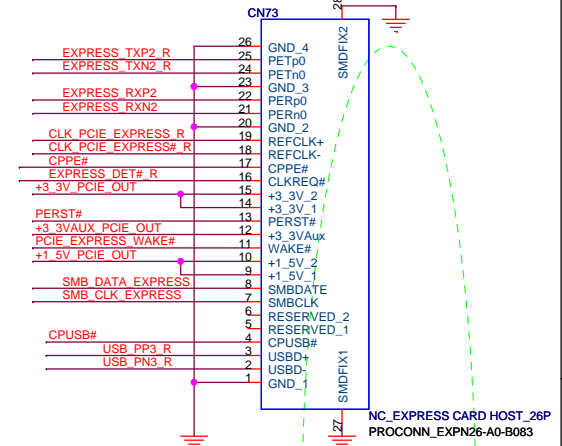
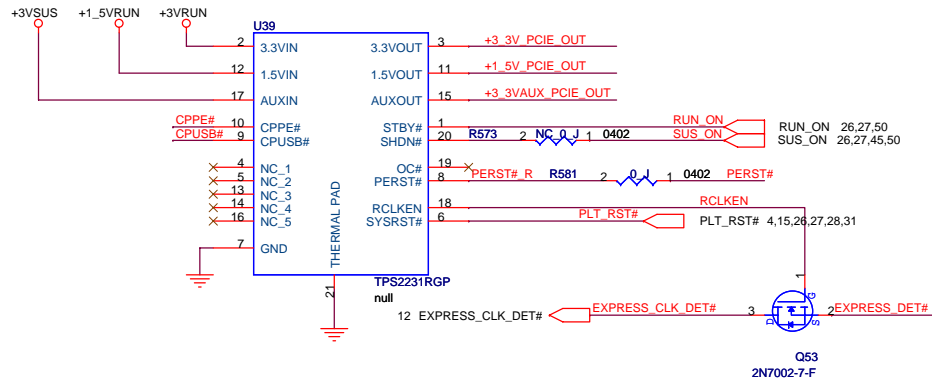






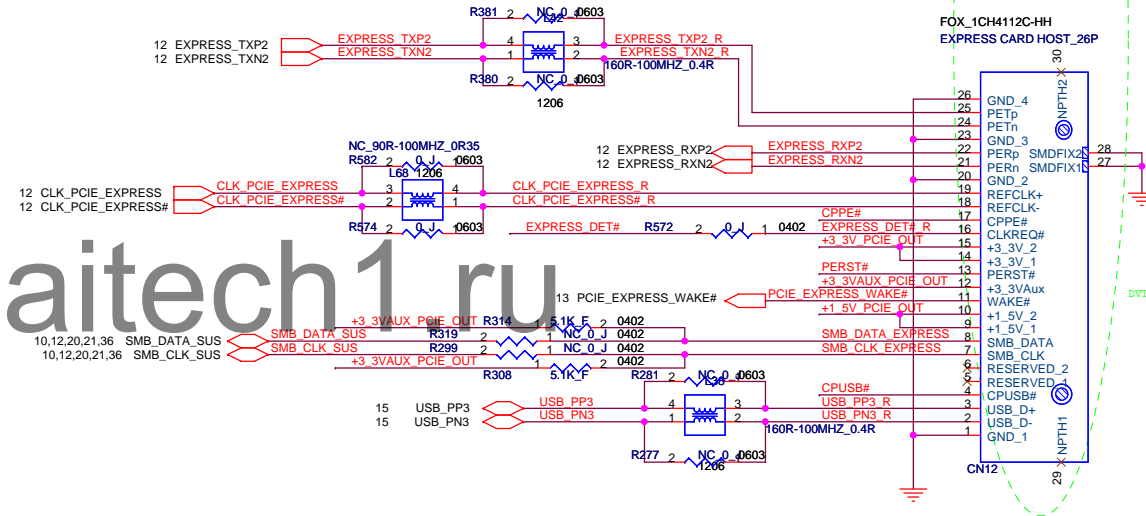
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+1_5V=>650mA
+3_3VAux=>275mA
+3_3V=>1.3A
Express Card Power Switch

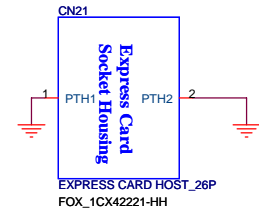


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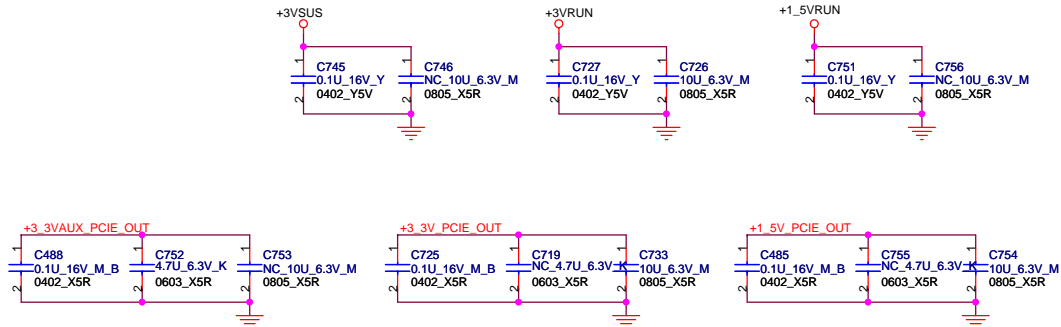
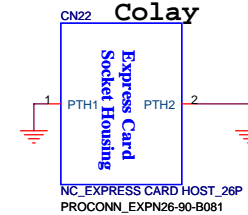
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EXPRESS CARD HOST_26P




Express Card Slot.

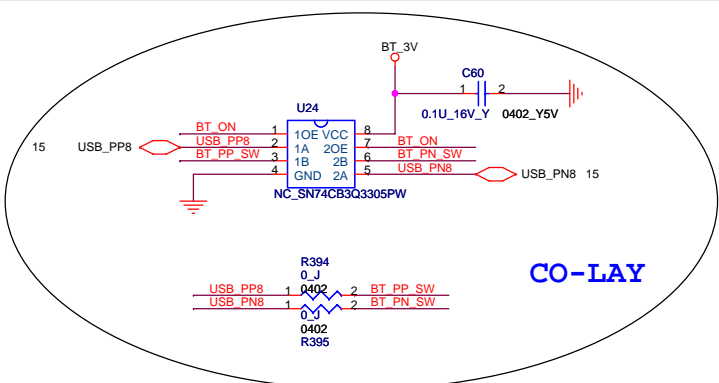


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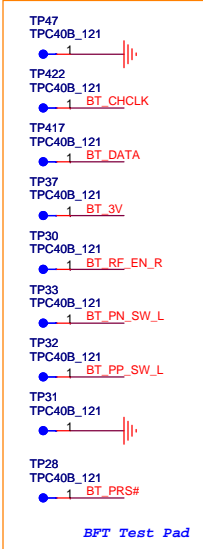
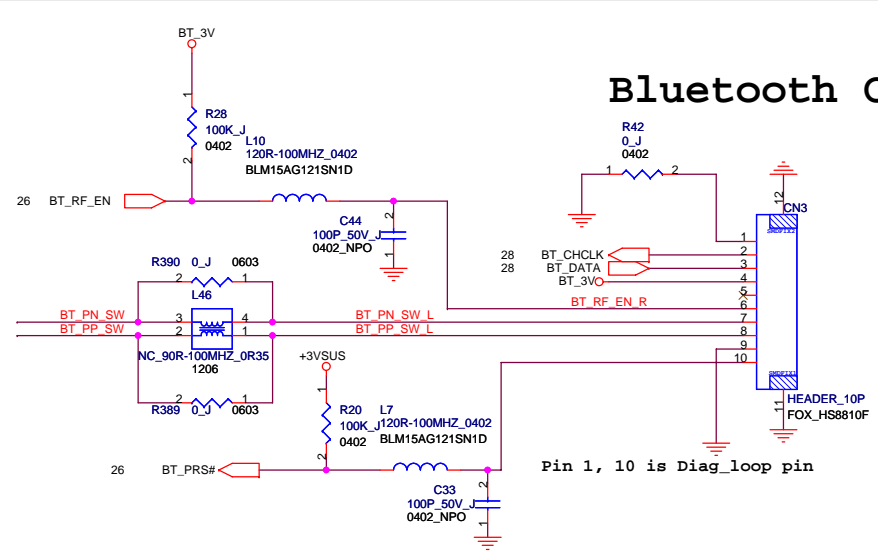
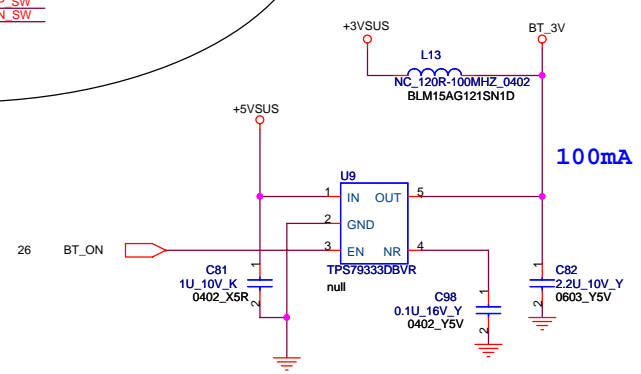



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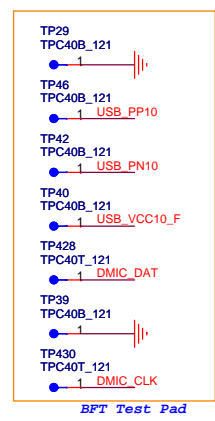
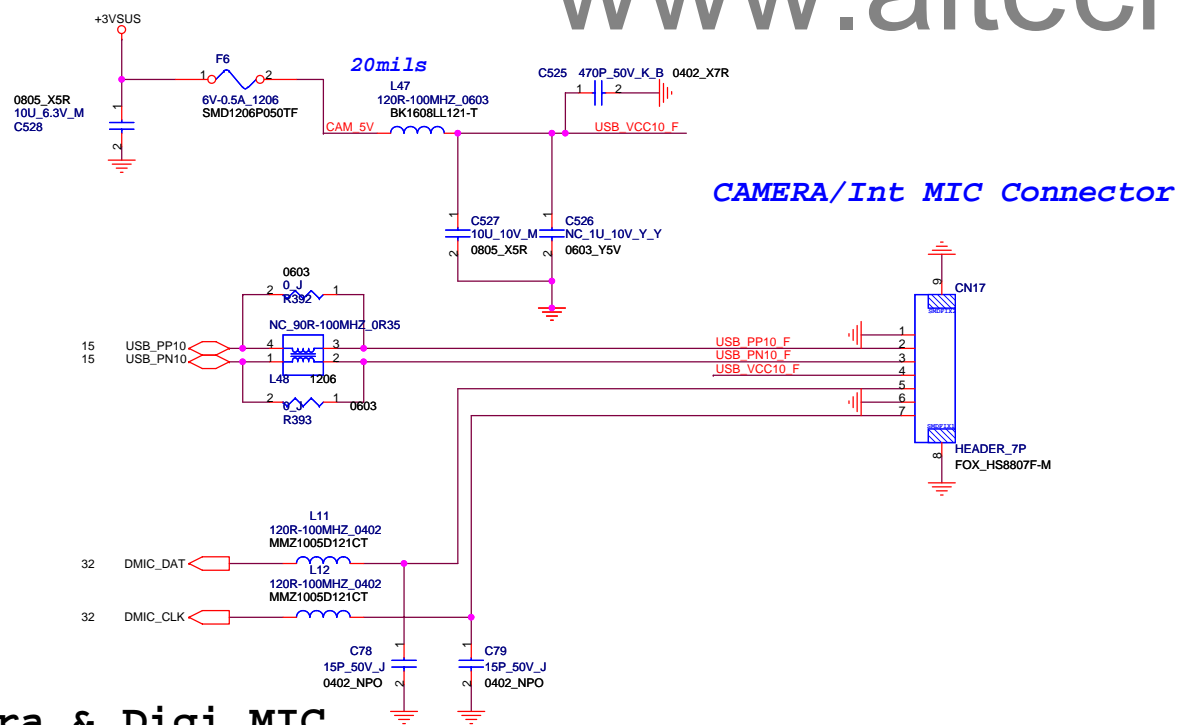
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Bluetooth



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Camera & Digi MIC

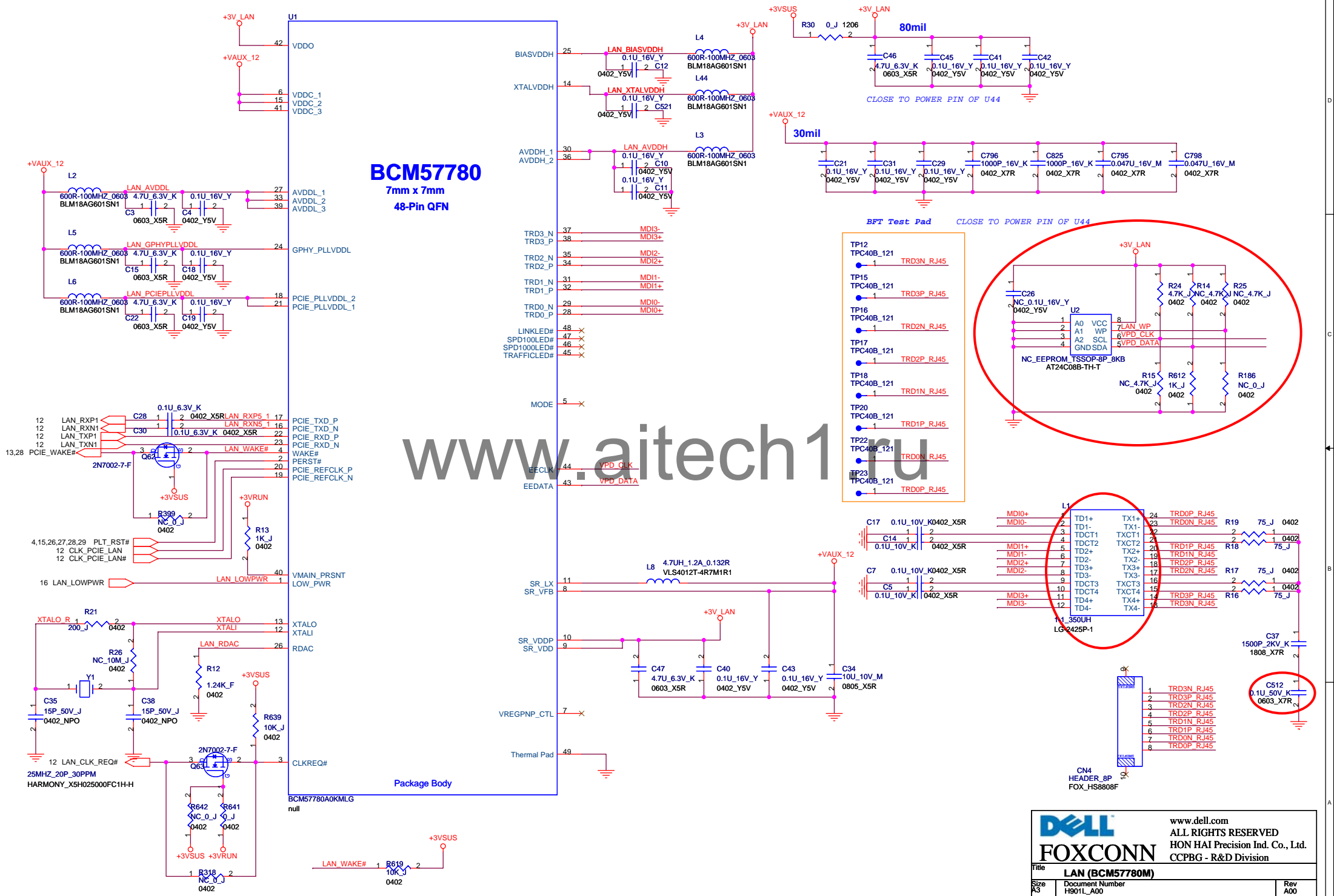
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Title BT & CAMERA/Dig MIC CON		
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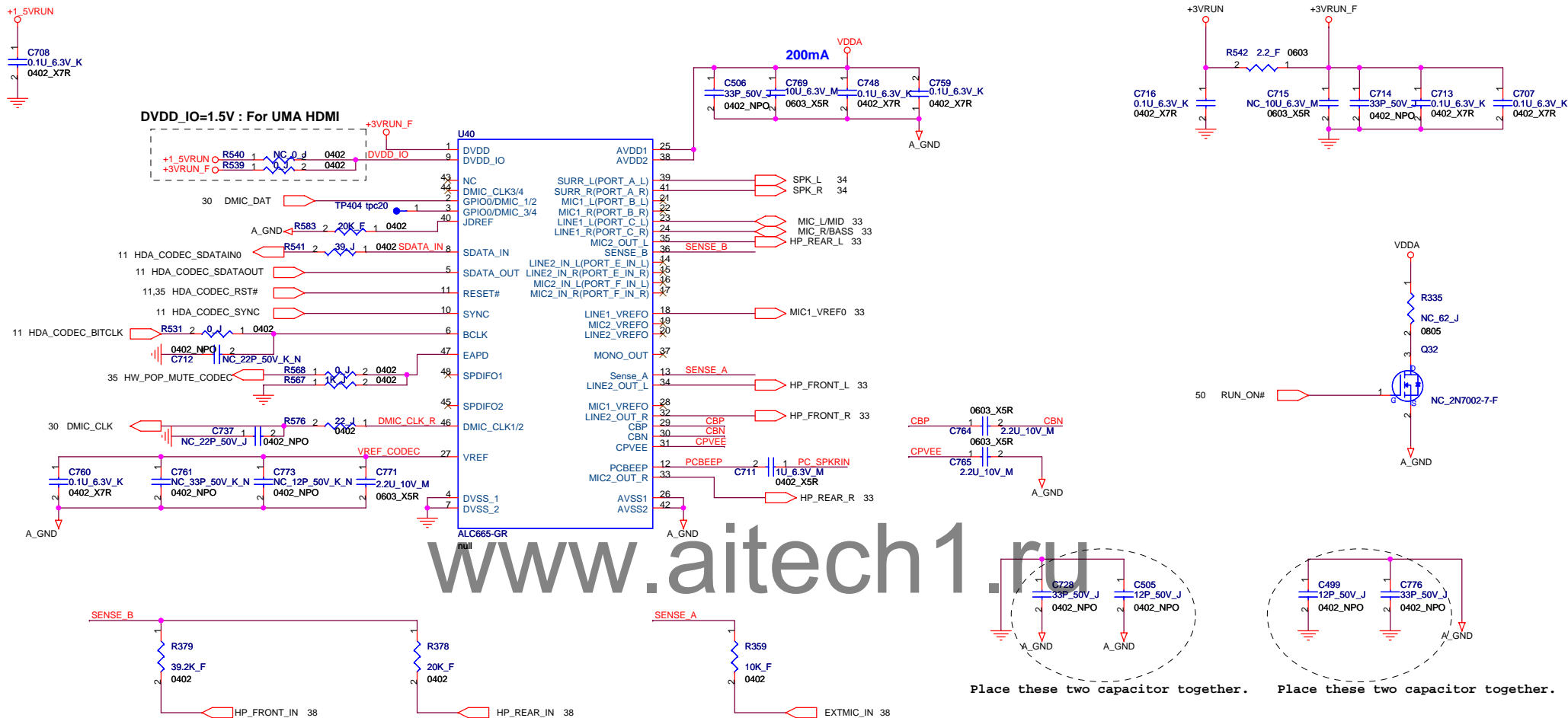
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LAN (BCM57780M)

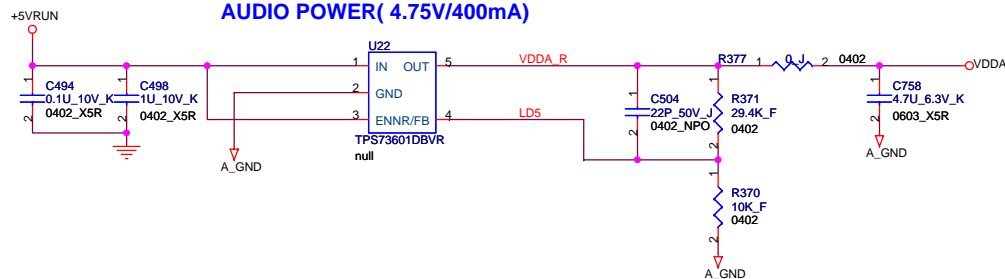
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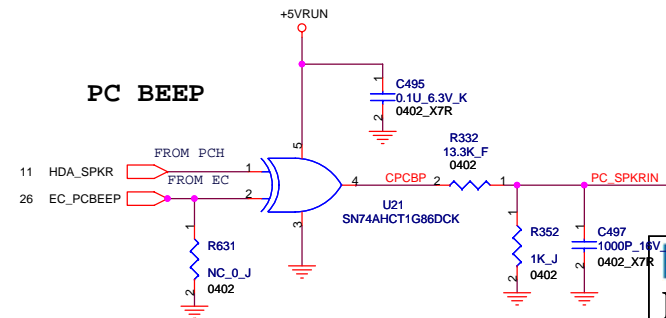
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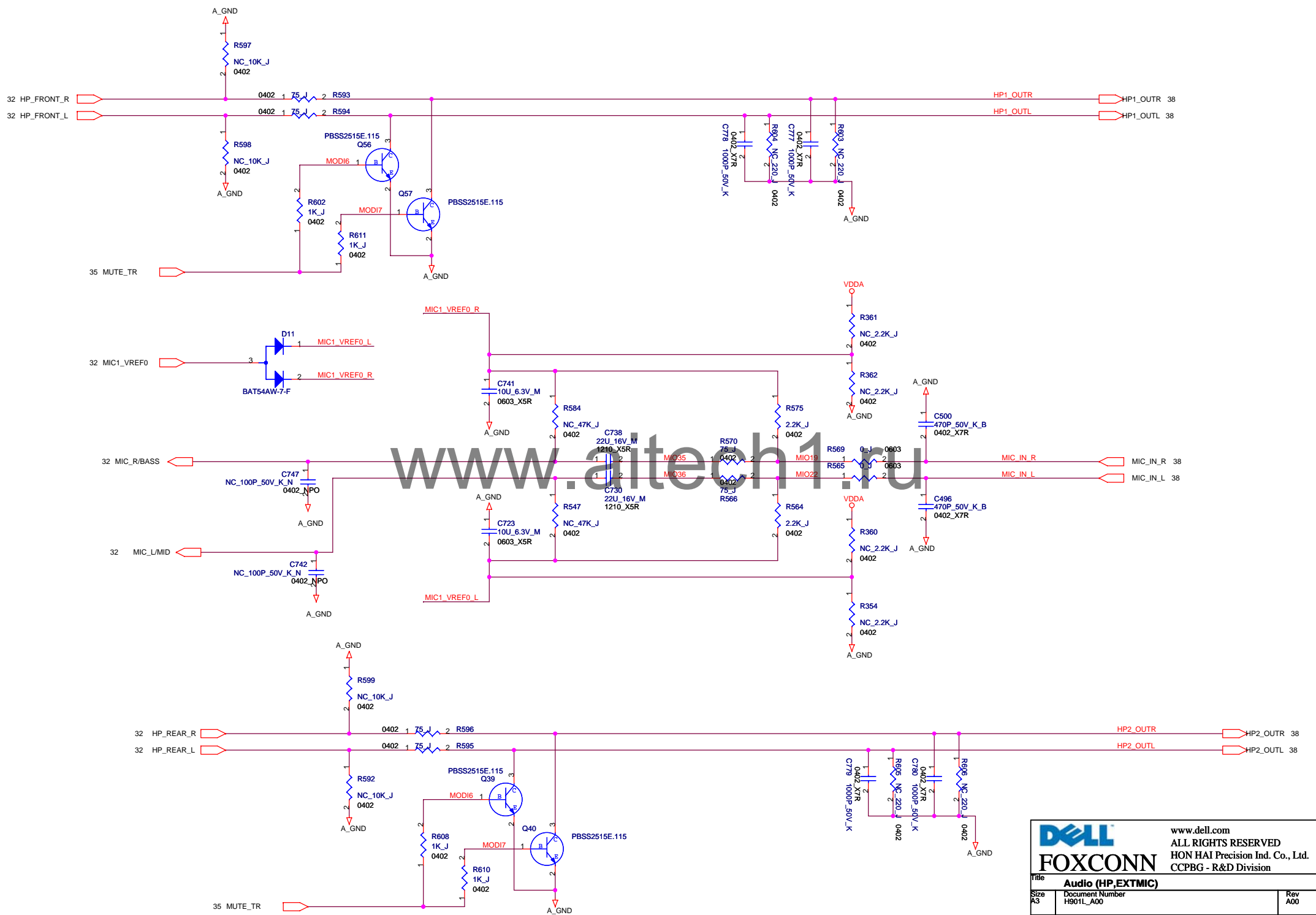
Place these two capacitor together.

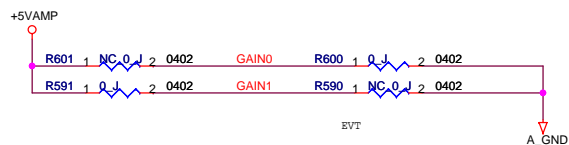
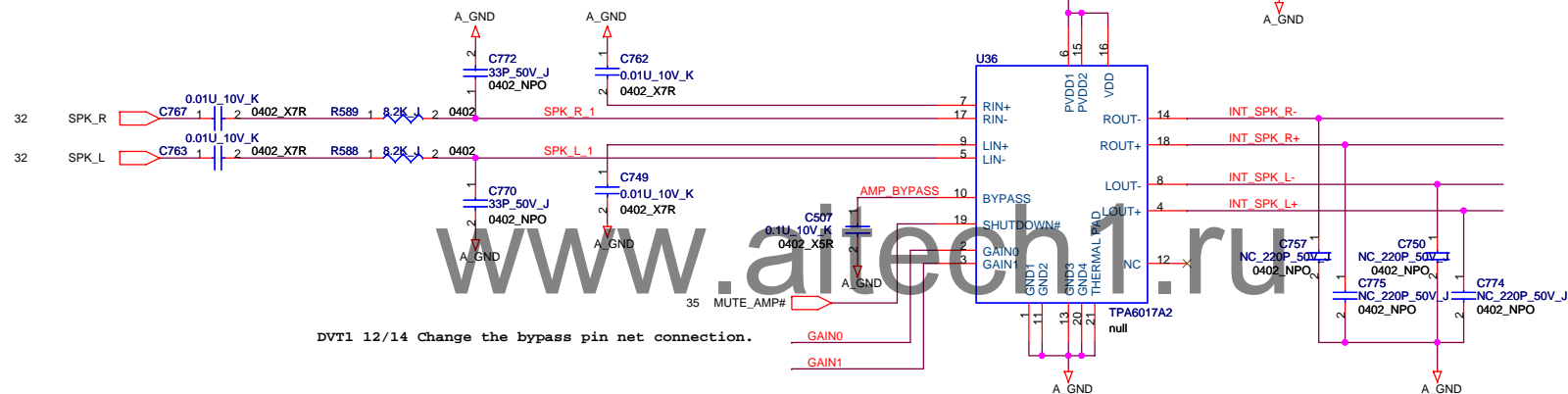
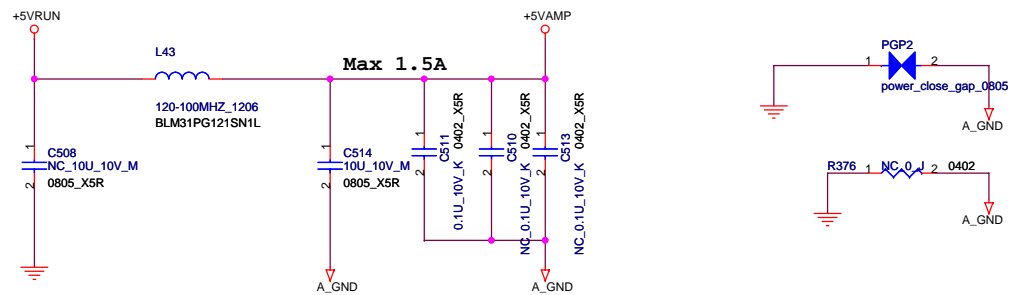
AUDIO POWER (4.75V/400mA)



PC BEEP



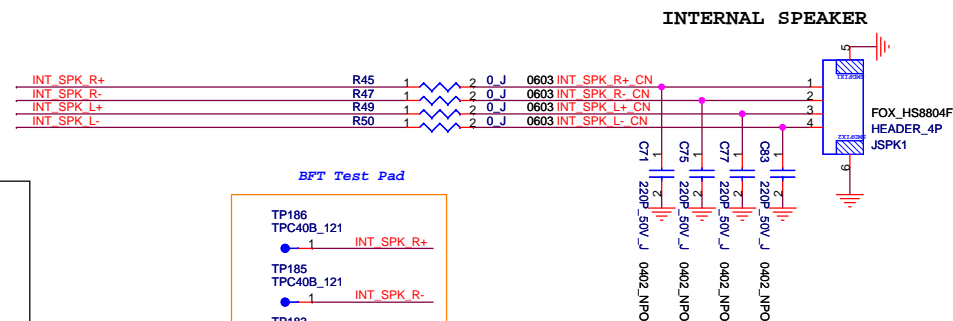


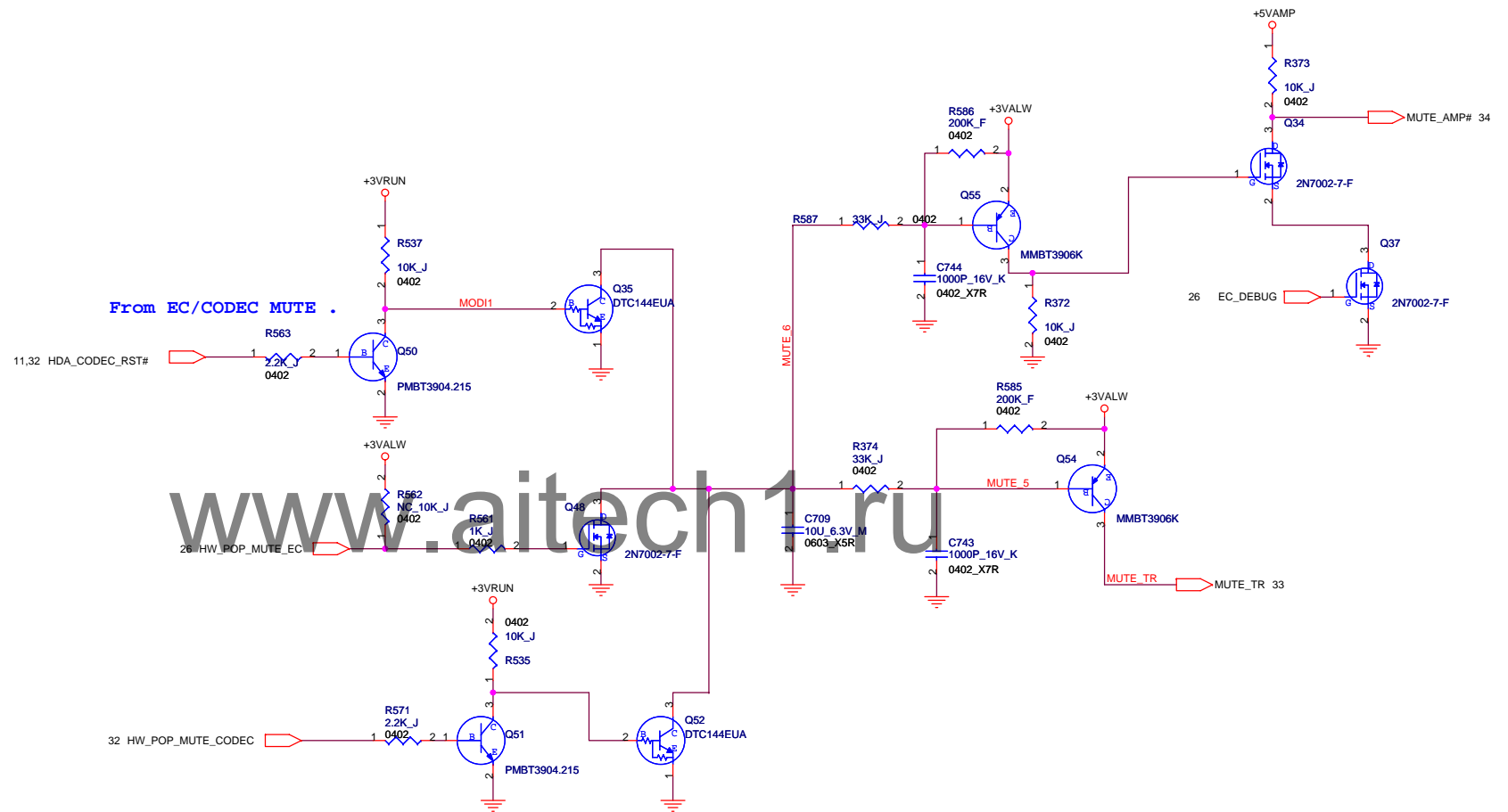


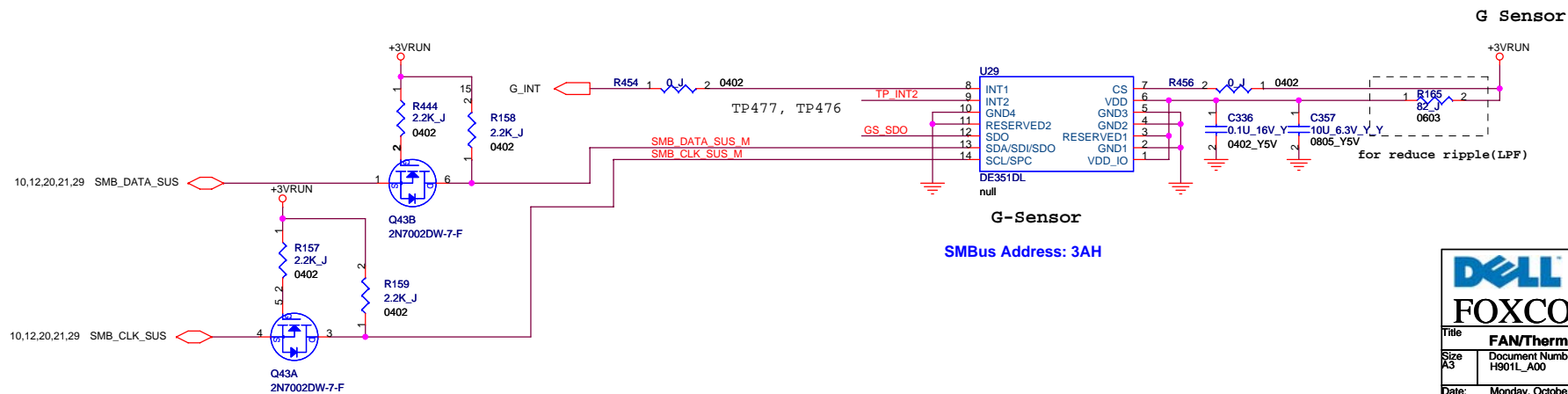
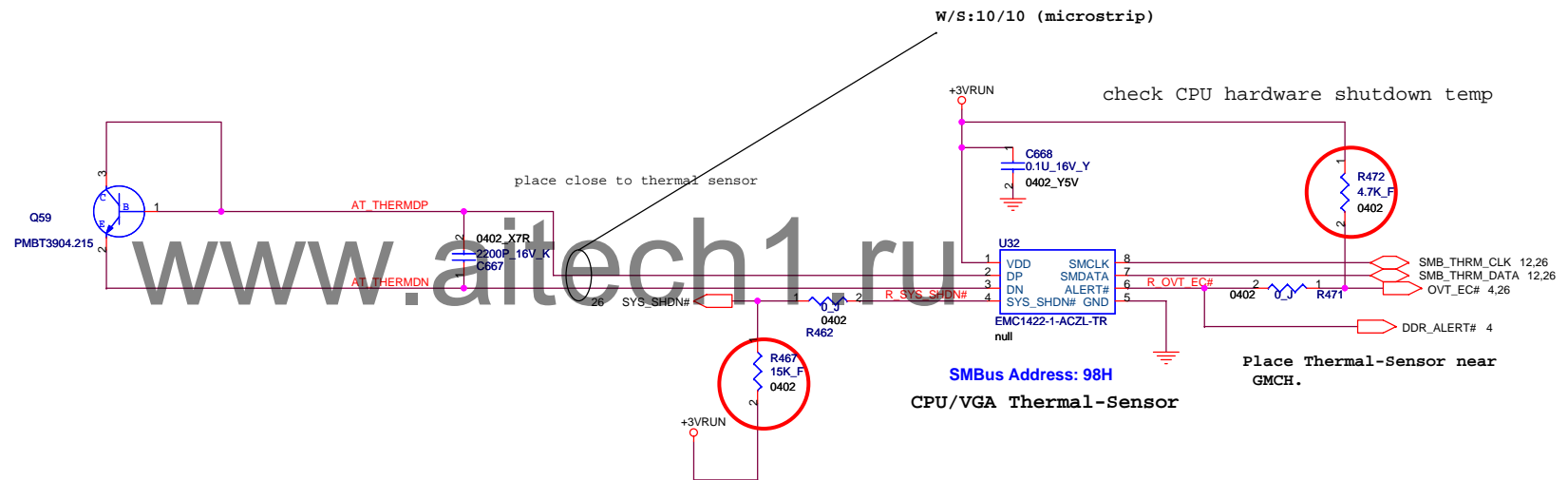
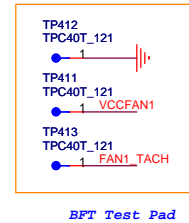
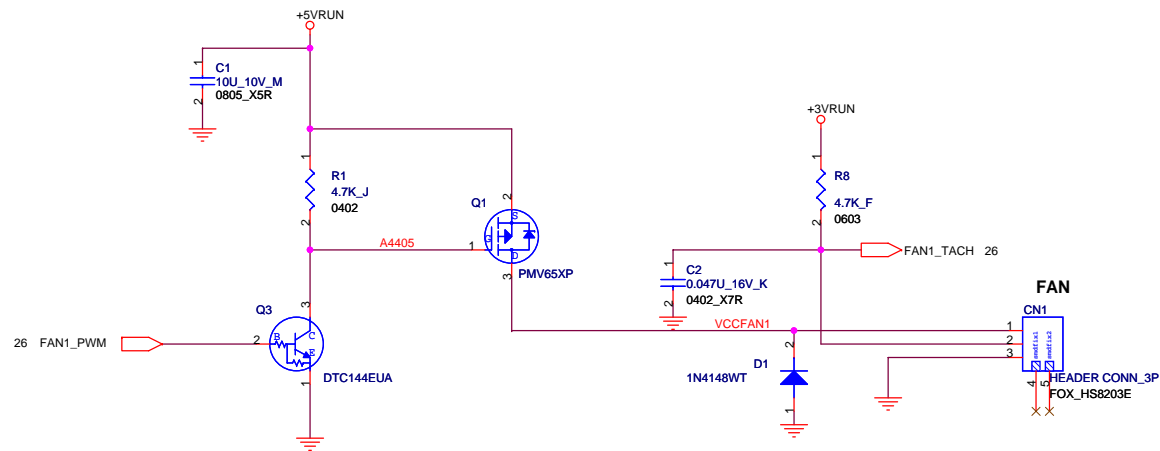
SPEAKER AMP

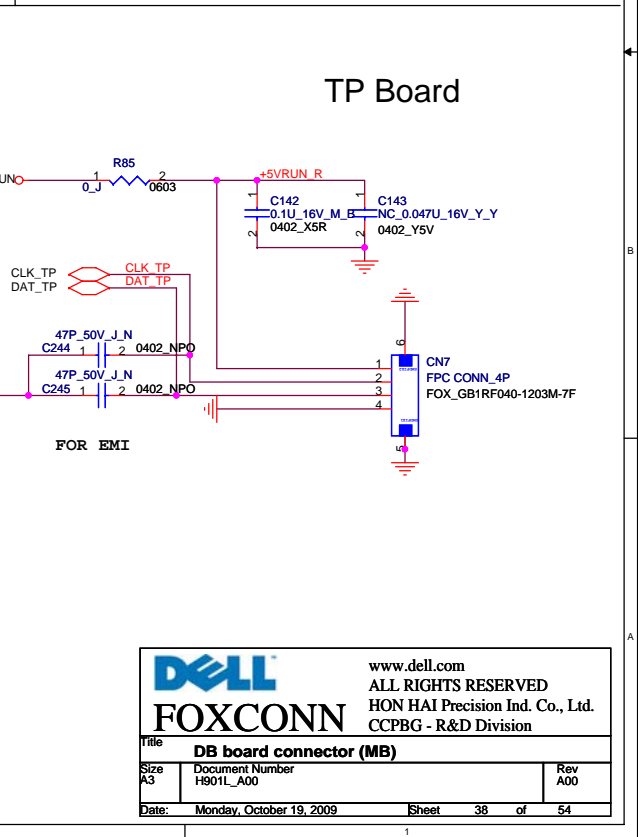
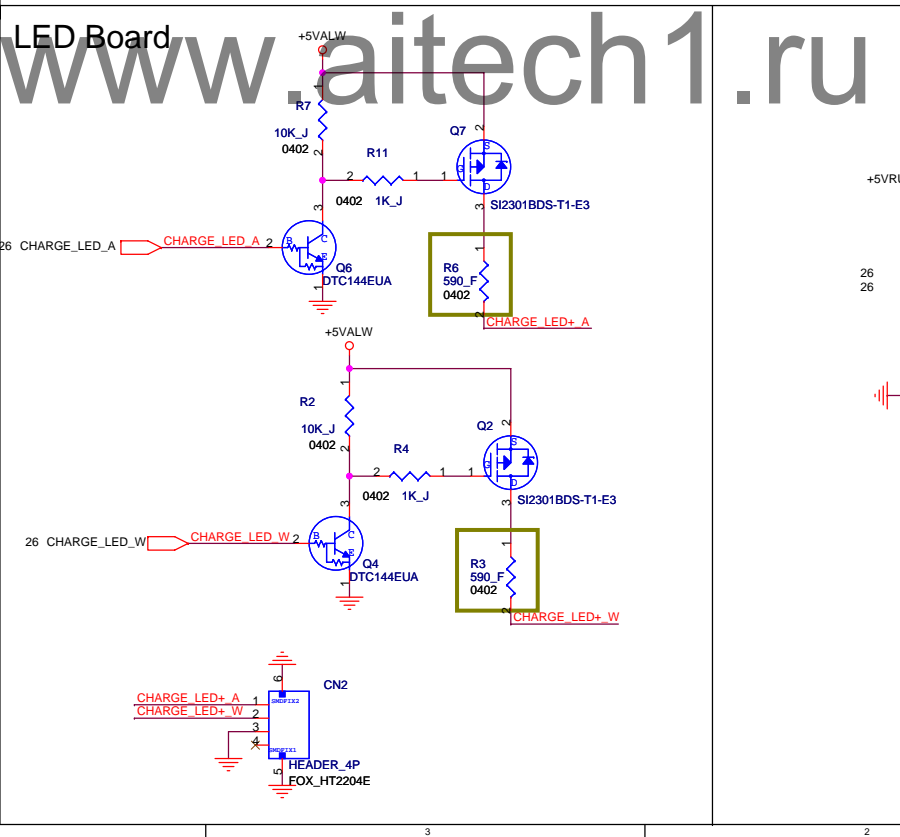
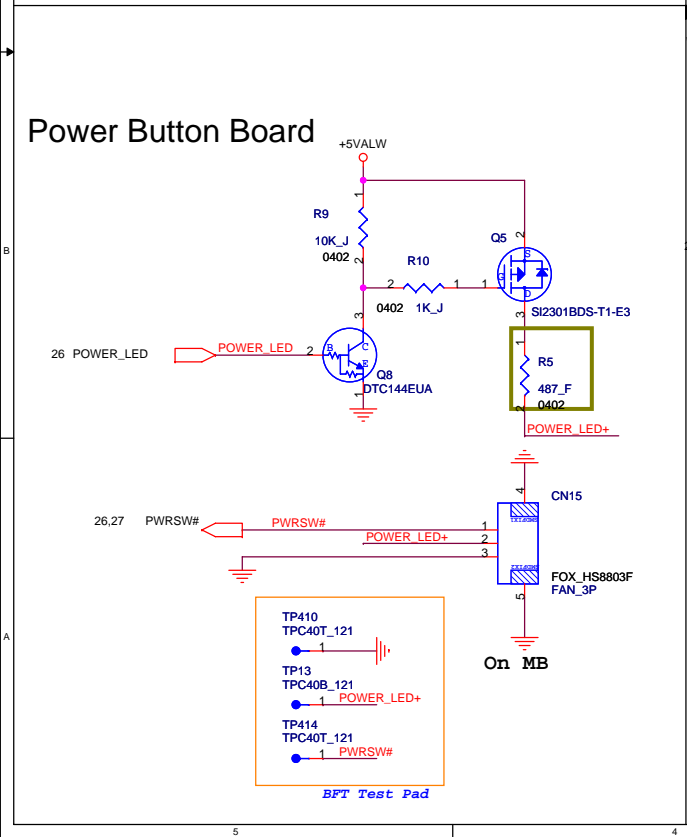
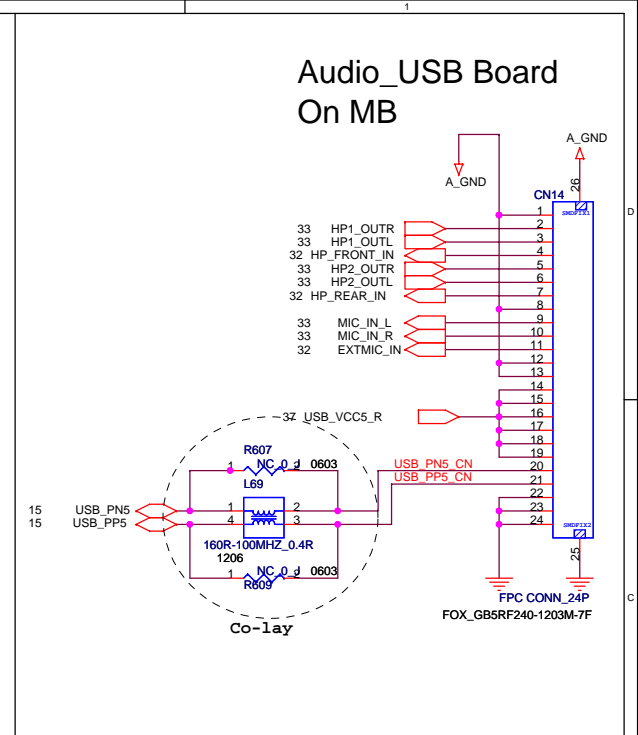
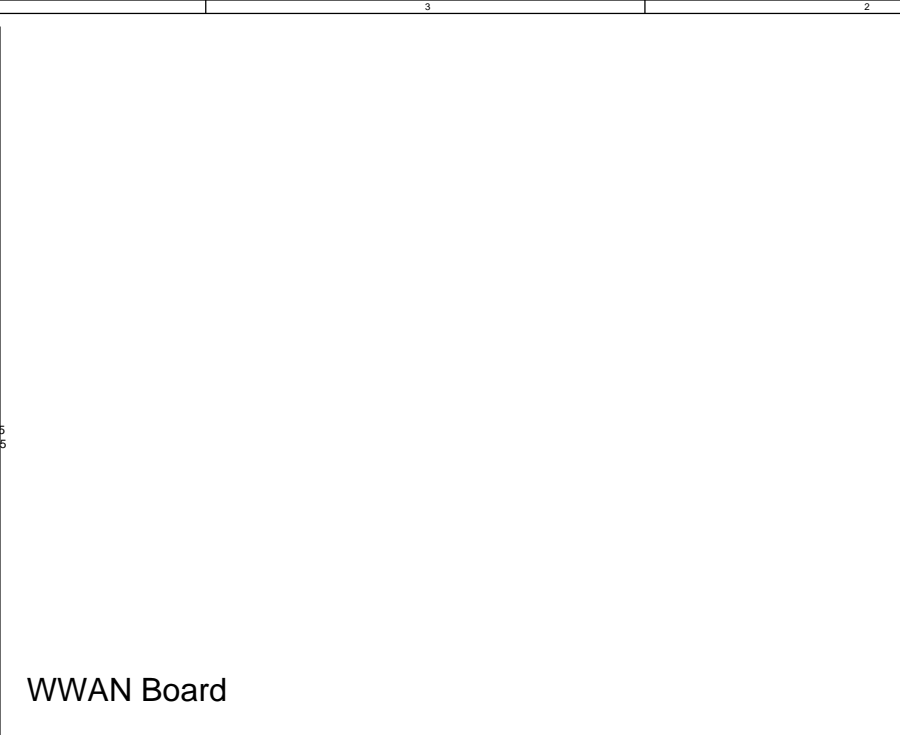
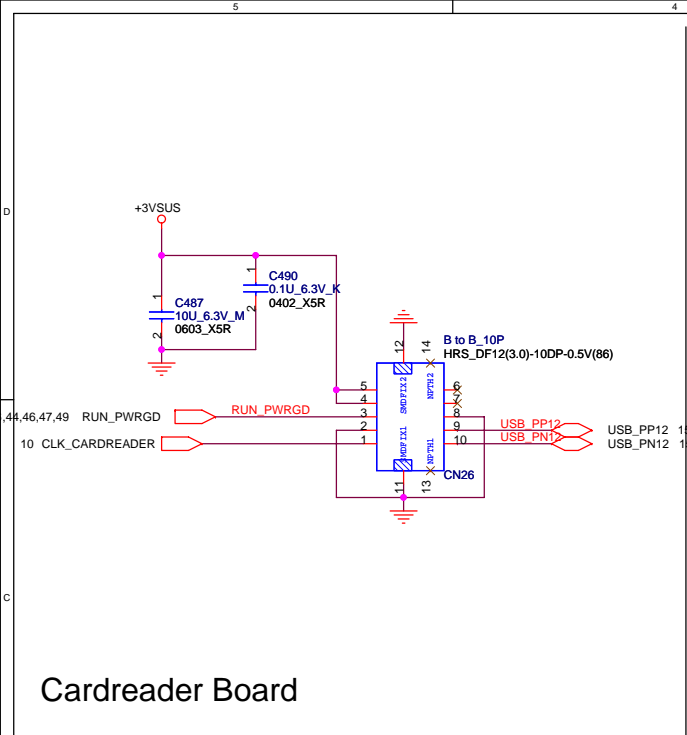
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

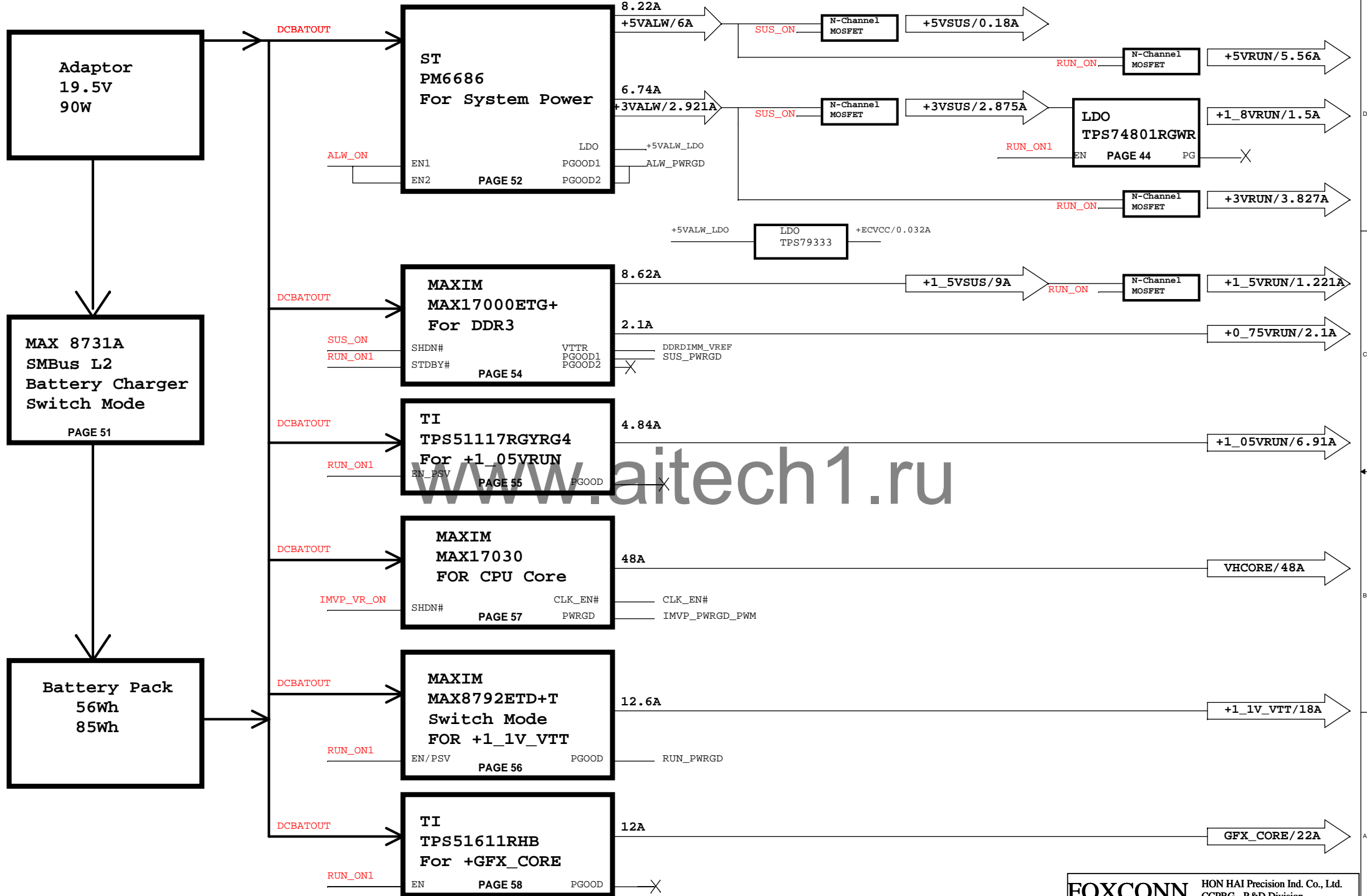
$dB = 20 \log \text{Gain}$
 If set 10dB, gain is 3.162.
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 \text{ W}$

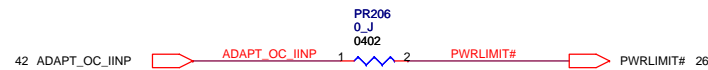
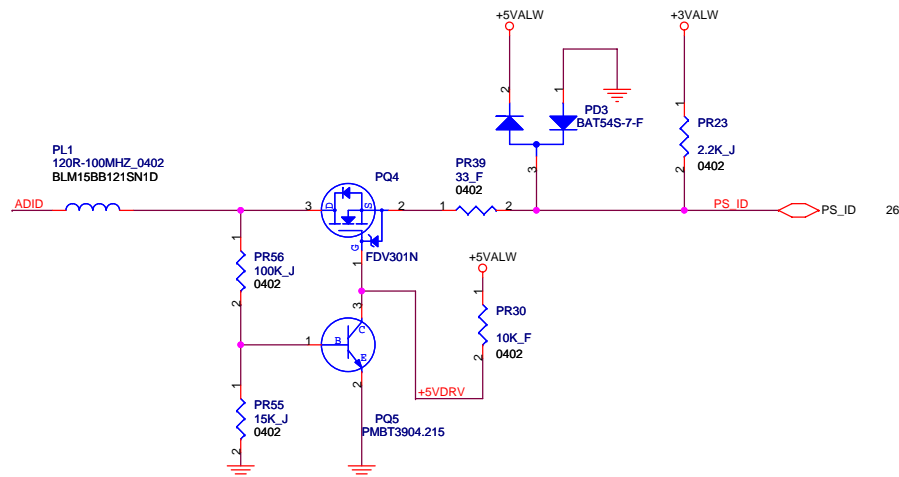
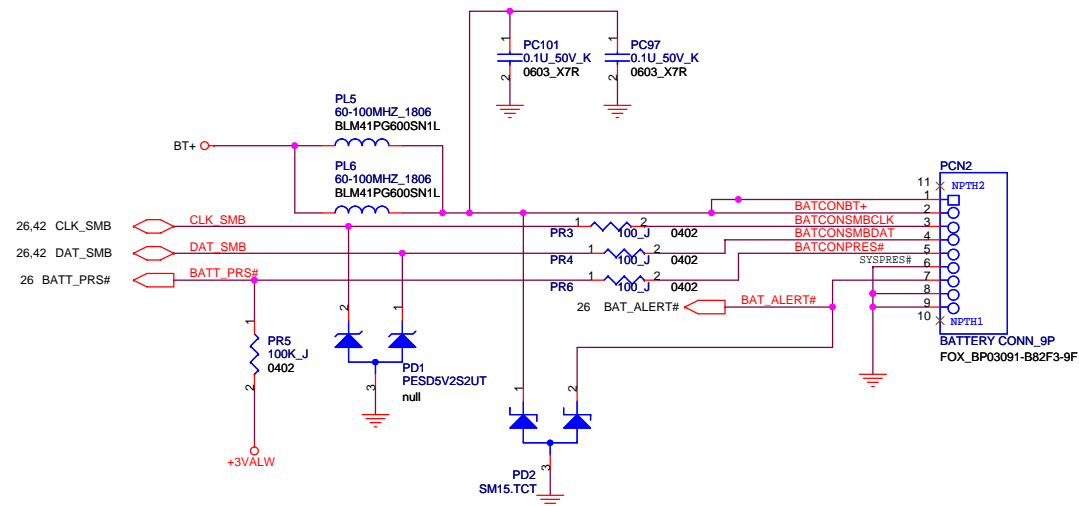
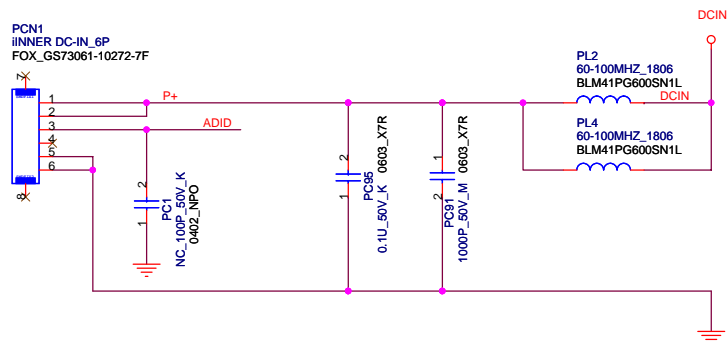
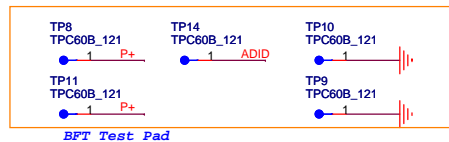




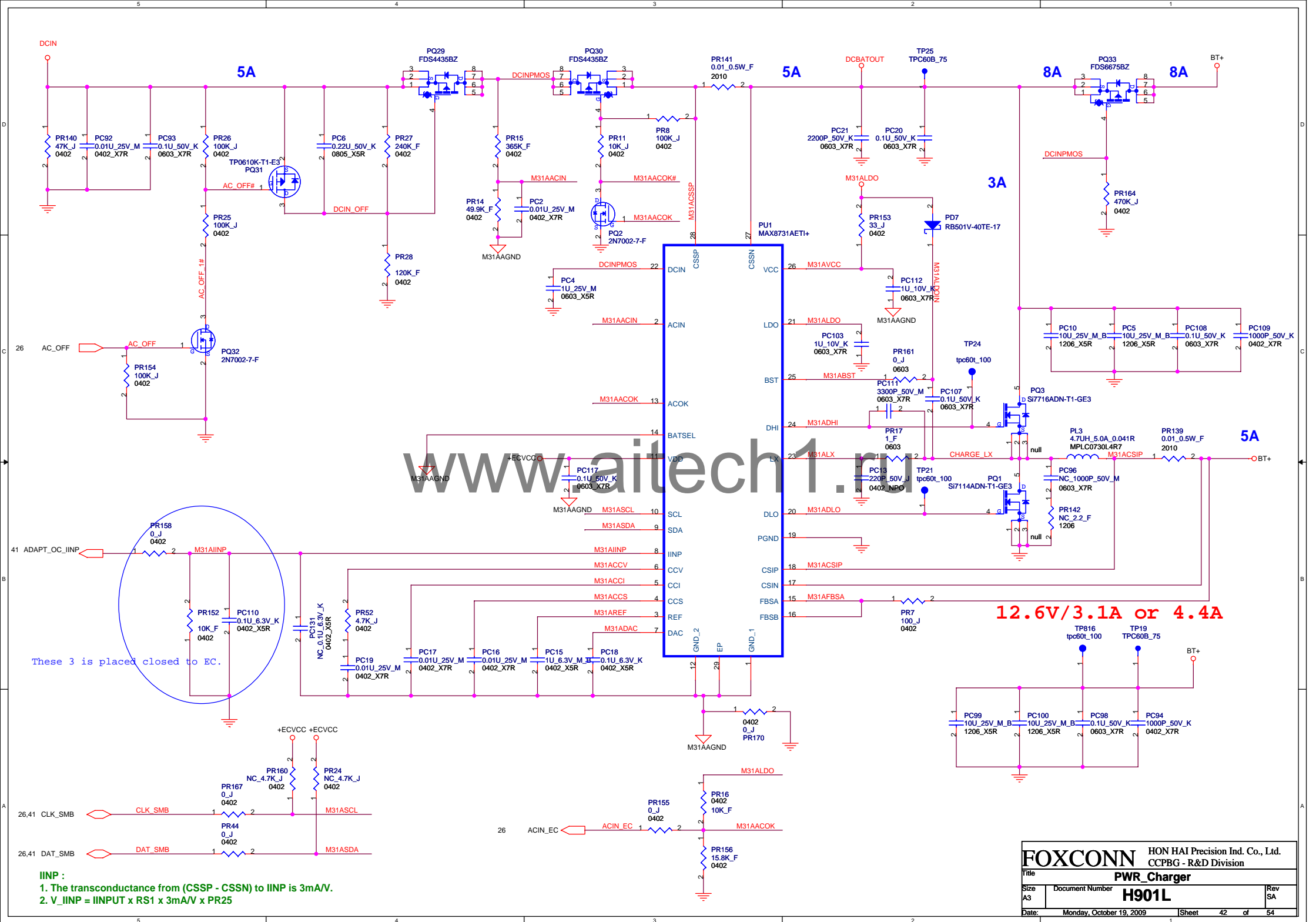


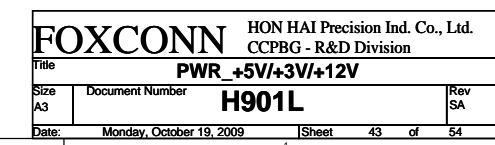






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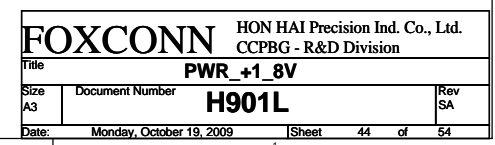


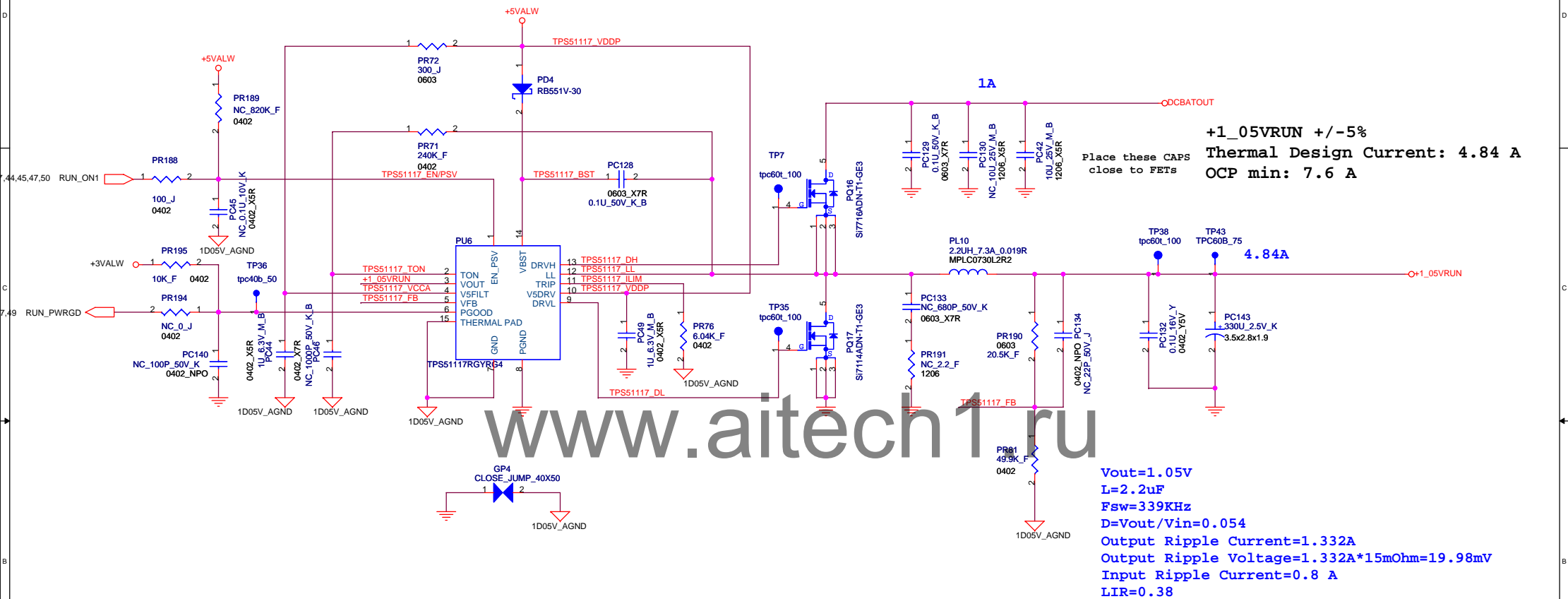
205
6.3V_K
03X7R

11 12 13 14 15

PU12
TPS74801RGWR

2
PR254
2.87K_F
0402

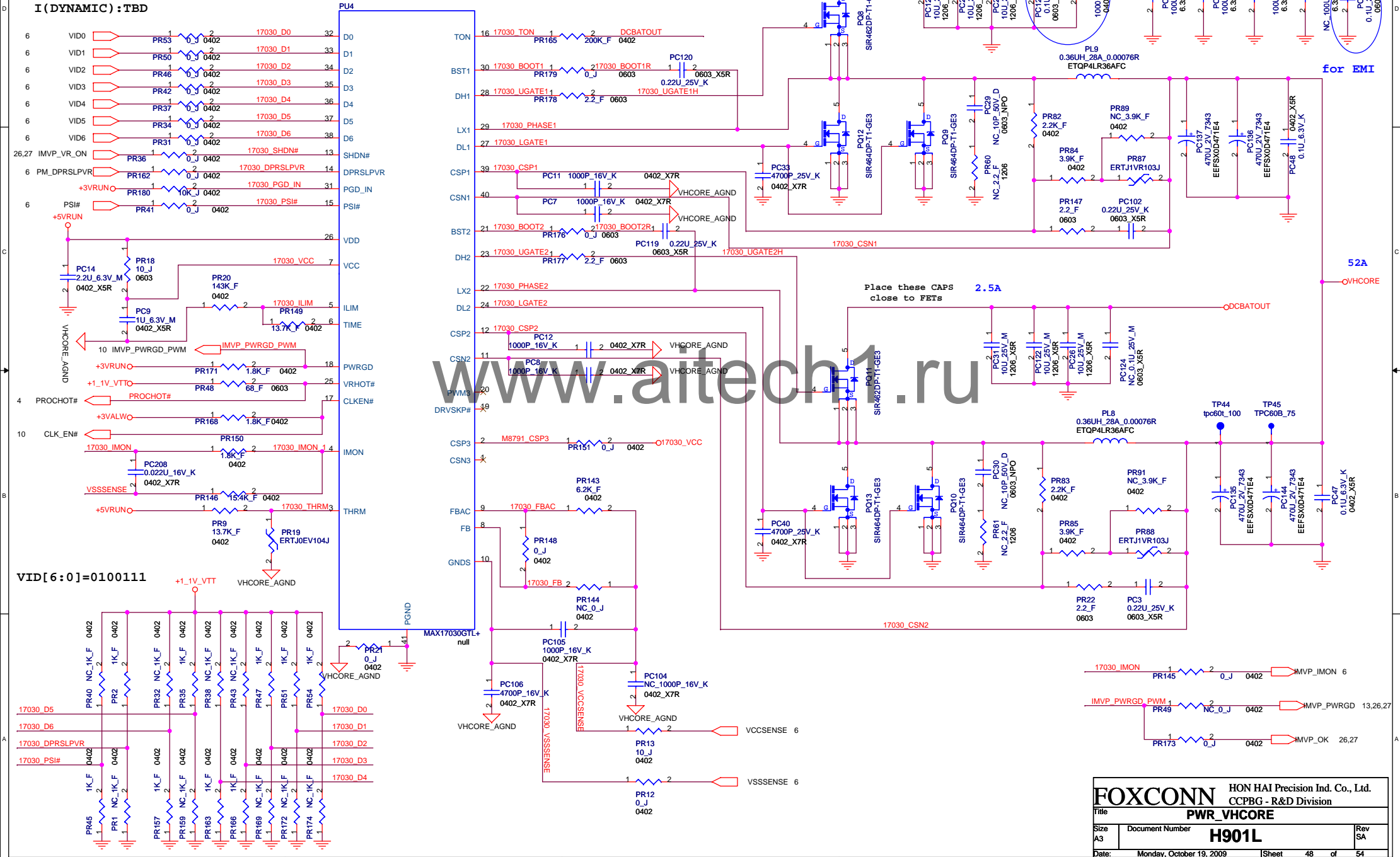


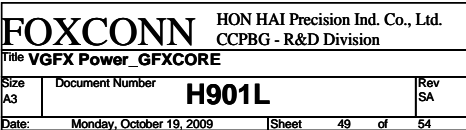


Arrandale SV CPU
V(HFM):0.95V
V(LFM):0.875V
LL:-1.9mOhm
Icc_max:48A
Icc_TDC:32 A
I(DYNAMIC):TBD

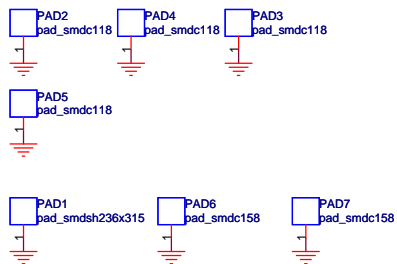
VID[5:3] for CSC, CRB default '100' = 50A (Iccmax)
VID[2:0] for MSID (To differentiate XE CPU from SV CPU)
DPRSLPVR='1' for IMVP6.5
Others are RSVD
Both PH and PD resistors are required to reserve for all 9 signals

OCP setting:60A(30A per phase).
PR149=13.7K Ohm

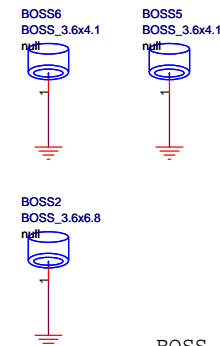
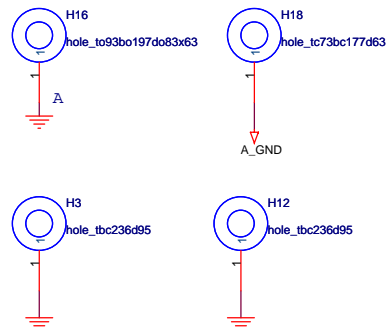




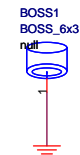
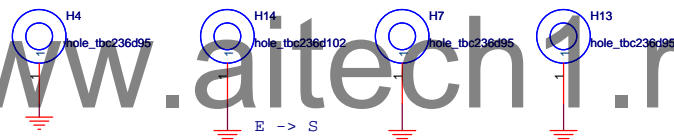
ME



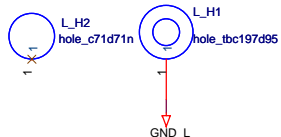
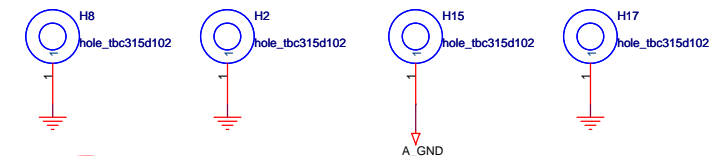
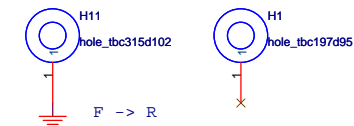
CPU



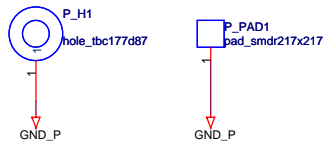
BOSS in Bottom side



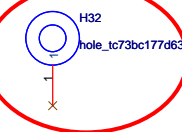
BOSS in Top side




LED



Power Button



For ME request.

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Title			
HOLE			
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H901L EVT

(2009/06/08)

P.39 Add Q62, Q63, R619, and R639 10K ohm and del D16 & D17 for leakage issue.

(2009/06/23)

P. 4 NC R712 0 ohm for DDR_alert# noise.

(2009/06/25)

P.11 Change RTC battery P/N from 1M-BCR2032-LB00 to 1M-BCR2032-LB01.

(2009/07/01)

P.51 Add H32 for ME request.

(2009/07/14)

P.12 Add R645 & R646 2.2K ohm for SMBUS PH.

P.31 Change C35 & C38 from 18pF to 15pF for Crystal vendor recommend.

(2009/07/15)

P.22 Add C655, C656, C657 10pF, and L70, L71, L72 47R, change L61, L62, L63 from 33R to 47R for CRT.

(2009/07/16)

P.13 Add R293 0 ohm NC for SLP_M#.

P.30 Change C33 and C44 from NPO 10% to 5% for PUR recommend.

P.39 Change P_C1, P_C2, L_C1, L_C2 from 10pF NPO 10% to 5% for PUR recommend.

P.32 Change C499 and C505 from 12pF NPO 10% to 5% for PUR recommend.

P.11 Change C735 from 12pF NPO 10% to 5% for PUR recommend.

P.30 Change C78 and C79 from 15pF NPO 10% to 5% for PUR recommend.

P.11 Change C736 from 15pF NPO 10% to 5% for PUR recommend.

P.38 Change C244 and C245 from 47pF NPO 10% to 5% for PUR recommend.

(2009/07/17)

P.13 Add R763 10K ohm PH for HDMI.

P.31 Add C512 0.1uF for Hipot test.

H901L DVT

(2009/07/23)

P.36 Change R467 from 33K to 15K ohm and R472 from 15K to 4.7K ohm for Thermal recommend.

(2009/07/28)

P.24 Change HDMI connector from 2N-0019003-FKG0 to 2N-0019002-MKG0

(2009/08/20)

P.28 Delete R27

P.31 Change L1 to LANKOM.

P.18 Delete R257

H901L PVT

(2009/09/3)

P. 20 & 21 Change CN27 & CN28 to tray for L6 recommend.

P. 25 Change CN25 & CN8 to tray for L6 recommend.

P. 29 Change CN73 Part number for CIS recommend.

P. 20 Add R27 & R55 1K ohm for Intel M1 DDR solution.

P. 21 Add R56 & R57 1K ohm for Intel M1 DDR solution.

H901L X-Build

(2009/09/16)

P.12 Change C701 & C702 from 18pF to 12pF for Crystal vendor recommend.

P.22 Add R474 0 ohm for EMI solution.

H901L X-Build

(2009/09/18)

P.31 Add R612 1K ohm .

P.31 Delete C26

P.31 Delete U2


P.31 Delete R14

P.31 Delete R186

(2009/10/14)

P.29 Add L38 , L42 & L69

P.29 Delete R277, R281, R380, R381, R607, R609 for EMI


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Title History (1)		
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H900 Power Change History

Number	Date	Page	Title	Issue	Description	Version
1	2009/07/02	P.48	V_CORE	Chage exposed GND and VDD capacitor of VCORE to PGND.	Change PC14.2 from AGND to PGND. Change PU4.41 from AGND to PGND. Change PR21.2 from PGND to AGND.	X01
2	2009/07/02	P.48	V_CORE	Add feedback capacitor to improve GND noise for system with battery only can't power ON issue.	Add PC7: 1000pF 16V X7R(1C-2B20102-K001) . Add PC8: 1000pF 16V X7R(1C-2B20102-K001) . Add PC11: 1000pF 16V X7R(1C-2B20102-K001) . Add PC12: 1000pF 16V X7R(1C-2B20102-K001) .	X01
3	2009/07/02	P.48	V_CORE	Change boost resistor to reduce ring of Mosfet.	Change PR178 from 0 Ohm 0603 5%(1R-0000000-J300) to 2.2 Ohm 0603 1%(1R-000022X-F300) Change PR177 from 0 Ohm 0603 5%(1R-0000000-J300) to 2.2 Ohm 0603 1%(1R-000022X-F300)	X01
4	2009/07/08	P.49	+GFX_CORE	Delete some capacitors from TI suggestion. Fine tune load line and IMON setting.	Del PC190,PC192,PC189,PC199,PC201. Change PR223 from 3K 0402 1%(1R-0000302-F200) to 1.2K 0402 1%(1R-0000122-F200) Change PR232 from 10K 0402 1%(1R-0000103-F200) to 45.3K 0402 1%(1R-0004532-F200) Change PC198 from 3300P 50V 0402 10%(1C-2B20332-K000) to 0.47uF 6.3V 0402 10%(1C-2B20474-K000)	X01
5	2009/07/08	P.48	V_CORE	Modify DCR feedback and IMON setting. Change L-S Mosfet to SIR464 to improve efficiency.	Change PR84 and PR85 from 1.69K 0402 1%(1R-0001691-F200) to 3.9K 0402 1%(1R-0003901-F200) Change PR150 from 10K 0402 1%(1R-0000103-F200)to 1.8K 0402 1%(1R-0000182-F200) Change PC208 from 0.1uF 6.3V 0402(1C-2B20104-K101) to 0.022uF 16V 0402 X7R (1C-2B20223-K000) Change PR146 from 12K 0402 1%(1R-0000123-F200) to 15.4K 0402 1%(1R-0001542-F200) Change PQ9,PQ10,PQ12,PQ13 from SIR466(17-SIR466D-PT00) to SIR464(17-SIR464D-PT00)	X01
6	2009/07/10	P.42	Charger	Slow down P-Mos turn on to reduce inrush current of AC adapter.	Change PR28 from 100K 0402 5%(1R-0000104-J200) to 120K 0402 1%(1R-0000124-F200)	X01
7	2009/07/16	P.49	+GFX_CORE	Add a L-S Mosfet for GFX_CORE	Add PQ56:FDMS7670 (17-FDMS767-0000)	X01
8	2009/07/16	P.49	+GFX_CORE	Change GFX_CORE setting from vender's suggestion	Change PR224 from 124K 0402 1%(1R-0001243-F200) to 249K 0402 1%(1R-0002493-F200) Change PU11.33 to PGND. Change PU11.1 to AGND. Add a reserve PR258 between PU11.26 to AGND. Change PR234 from 82.5K 0402 1%(1R-0008252-F200) to 52.3K 0402 1%(1R-0005232-F200) Change PR242 from 63.4K 0402 1%(1R-0006342-F200) to 62K 0402 1%(1R-0000623-F200) Change PR239 from 51K 0402 1%(1R-0000513-F200) to 68K 0402 1%(1R-0000683-F200) Change PR223 from 1.2K 0402 1% (1R-0000122-F200) to 910 0402 1%(1R-0000911-F200)	X01
9	2009/07/20	P.50	Other power plane	Add discharge path for 1_5VRUN and 1_05VRUN	Add PR104:330 Ohm 0603 5%(1R-0000331-J300) Add PR95:330 Ohm 0603 5%(1R-0000331-J300) Add PQ21:2N7002-7-F SOT-23(17-2N70027-F000) Add PQ18:2N7002-7-F SOT-23(17-2N70027-F000)	X01

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